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SECTION 1. SUMMARY

☐ SERVICING PRECAUTIONS

❶ Always disconnect the power source before:

- 1) Removing or reinstalling any component, circuit board, module or any other instrument assembly.
- 2) Disconnecting or reconnecting any instrument electrical plug or other electrical connection.
- 3) Connecting a test substitute in parallel with an electrolytic capacitor in the instrument.

CAUTION: A wrong part substitution or incorrect polarity installation of electrolytic capacitors may result in an explosion hazard.

❷ Do not defeat any plug/socket B+ voltage interlocks with which instruments covered by this service manual might be equipped.

❸ Do not apply power to this instrument and or any of its electrical assemblies unless all solid-state device heat sinks are correctly installed.

❹ Always connect a test instrument's ground lead to the instrument chassis ground before connecting the test instrument positive lead. Always remove the test instrument ground lead last.

- 1) The service precautions are indicated or printed on the cabinet, chassis or components. When servicing, follow the printed or indicated service precautions and service materials.
- 2) The Components used in the unit have a specified conflammability and dielectric strength. When replacing any components, use components which have the same ratings. Components marked in the circuit diagram are important for safety or for the characteristics of the unit. Always replace with the exact components.
- 3) An insulation tube or tape is sometimes used and some components are raised above the printed writing board for safety. The internal wiring is sometimes clamped to prevent contact with heating components. Install them as they were.
- 4) After servicing always check that the removed screws, components and wiring have been installed correctly and that the portion around the service part has not been damaged. Further check the insulation between the blades of attachment plug and accessible conductive parts.

ESD PRECAUTIONS

Electrostatically Sensitive Devices (ESD)

Some semiconductor (solid state) devices can be damaged easily by static electricity. Such components commonly are called Electrostatically Sensitive Devices (ESD). Examples of typical ESD devices are integrated circuits and some field-effect transistors and semiconductor chip components. The following techniques should be used to help reduce the incidence of component damage caused by static electricity.

1. Immediately before handling any semiconductor component or semiconductor-equipped assembly, drain off any electrostatic charge on your body by touching a known earth ground. Alternatively, obtain and wear a commercially available discharging wrist strap device, which should be removed for potential shock reasons prior to applying power to the unit under test.
2. After removing an electrical assembly equipped with ESD devices, place the assembly on a conductive surface such as aluminum foil, to prevent electrostatic charge buildup or exposure of the assembly.
3. Use only a grounded-tip soldering iron to solder or unsolder ESD devices.
4. Use only an anti-static solder removal device. Some solder removal devices not classified as "anti-static" can generate electrical charges sufficient to damage ESD devices.
5. Do not use freon-propelled chemicals. These can generate electrical charges sufficient to damage ESD devices.
6. Do not remove a replacement ESD device from its protective package until immediately before you are ready to install it. (Most replacement ESD devices are packaged with leads electrically shorted together by conductive foam, aluminum foil or comparable conductive materials).
7. Immediately before removing the protective material from the leads of a replacement ESD device, touch the protective material to the chassis or circuit assembly into which the device will be installed.

CAUTION : BE SURE NO POWER IS APPLIED TO THE CHASSIS OR CIRCUIT, AND OBSERVE ALL OTHER SAFETY PRECAUTIONS.

8. Minimize bodily motions when handing unpackaged replacement ESD devices. (Otherwise harmless motion such as the brushing together of your clothes fabric or the lifting of your foot from a carpeted floor can generate static electricity sufficient to damage an ESD device).

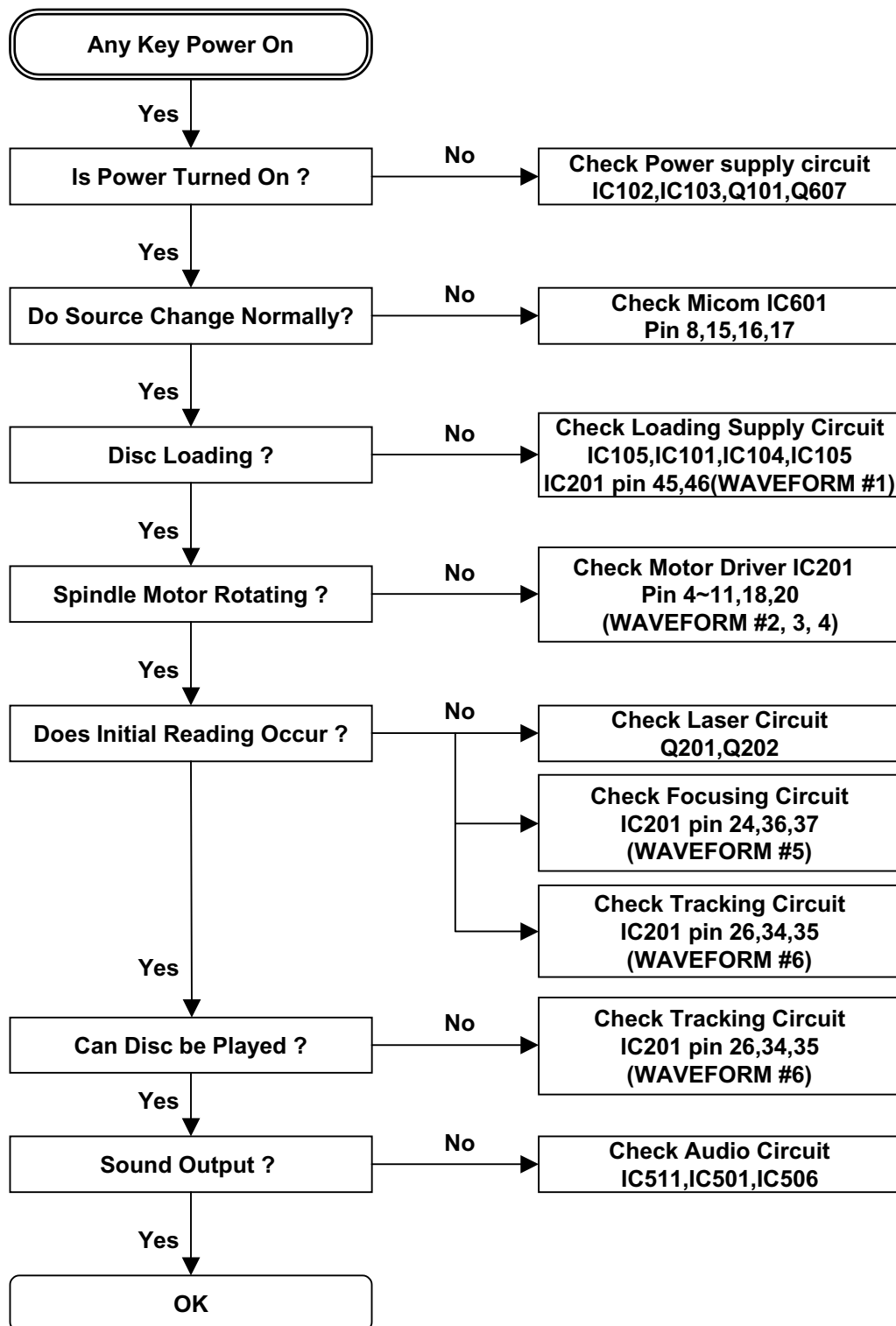
CAUTION. GRAPHIC SYMBOLS

	THE LIGHTNING FLASH WITH APROWHEAD SYMBOL. WITHIN AN EQUILATERAL TRIANGLE, IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF UNINSULATED "DANGEROUS VOLTAGE" THAT MAY BE OF SUFFICIENT MAGNITUDE TO CONSTITUTE A RISK OF ELECTRIC SHOCK.
	THE EXCLAMATION POINT WITHIN AN EQUILATERAL TRIANGLE IS INTENDED TO ALERT THE SERVICE PERSONNEL TO THE PRESENCE OF IMPORTANT SAFETY INFORMATION IN SERVICE LITERATURE.

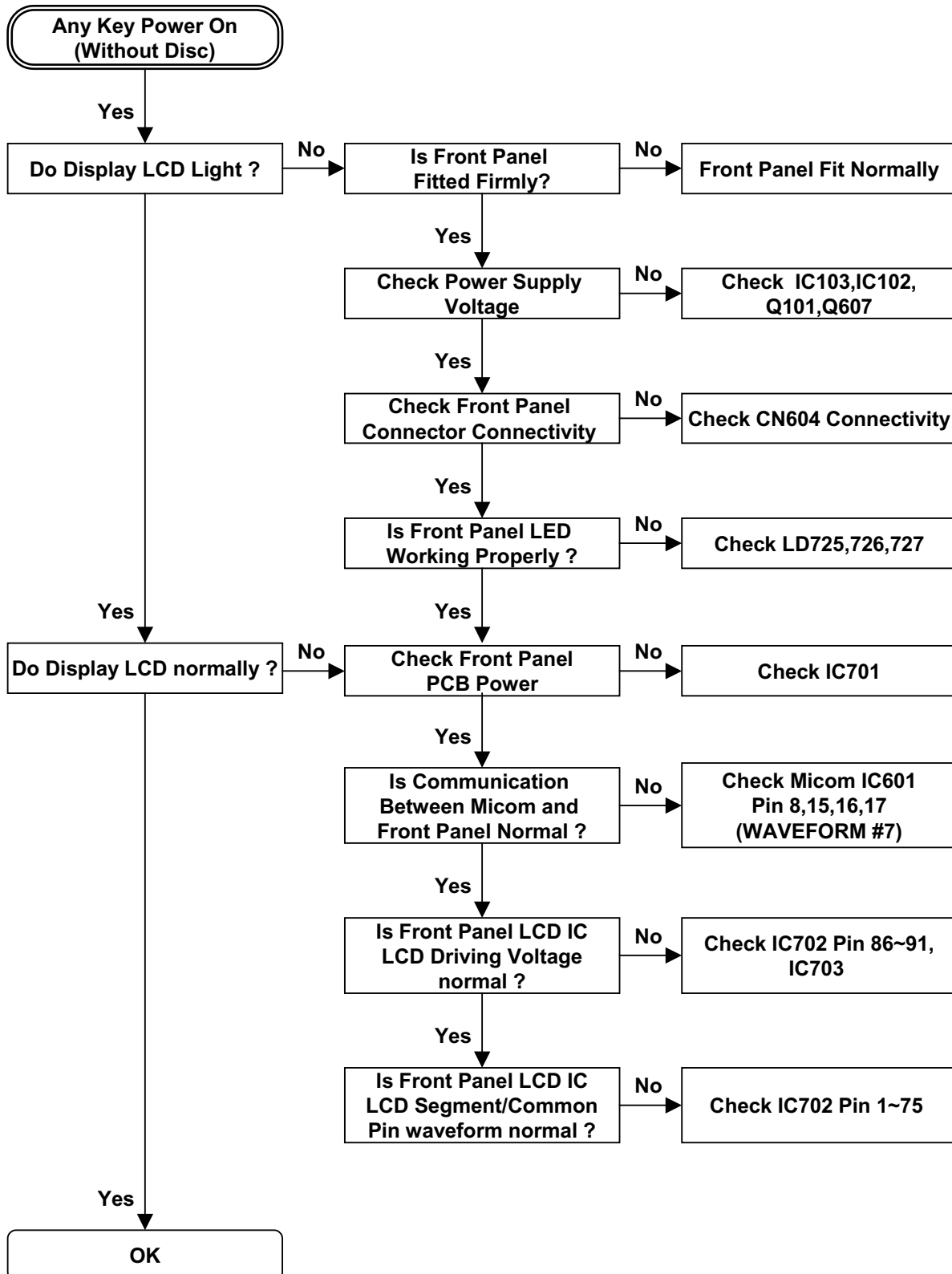
SECTION 2. ELECTRICAL

□ ELECTRICAL TROUBLESHOOTING GUIDE

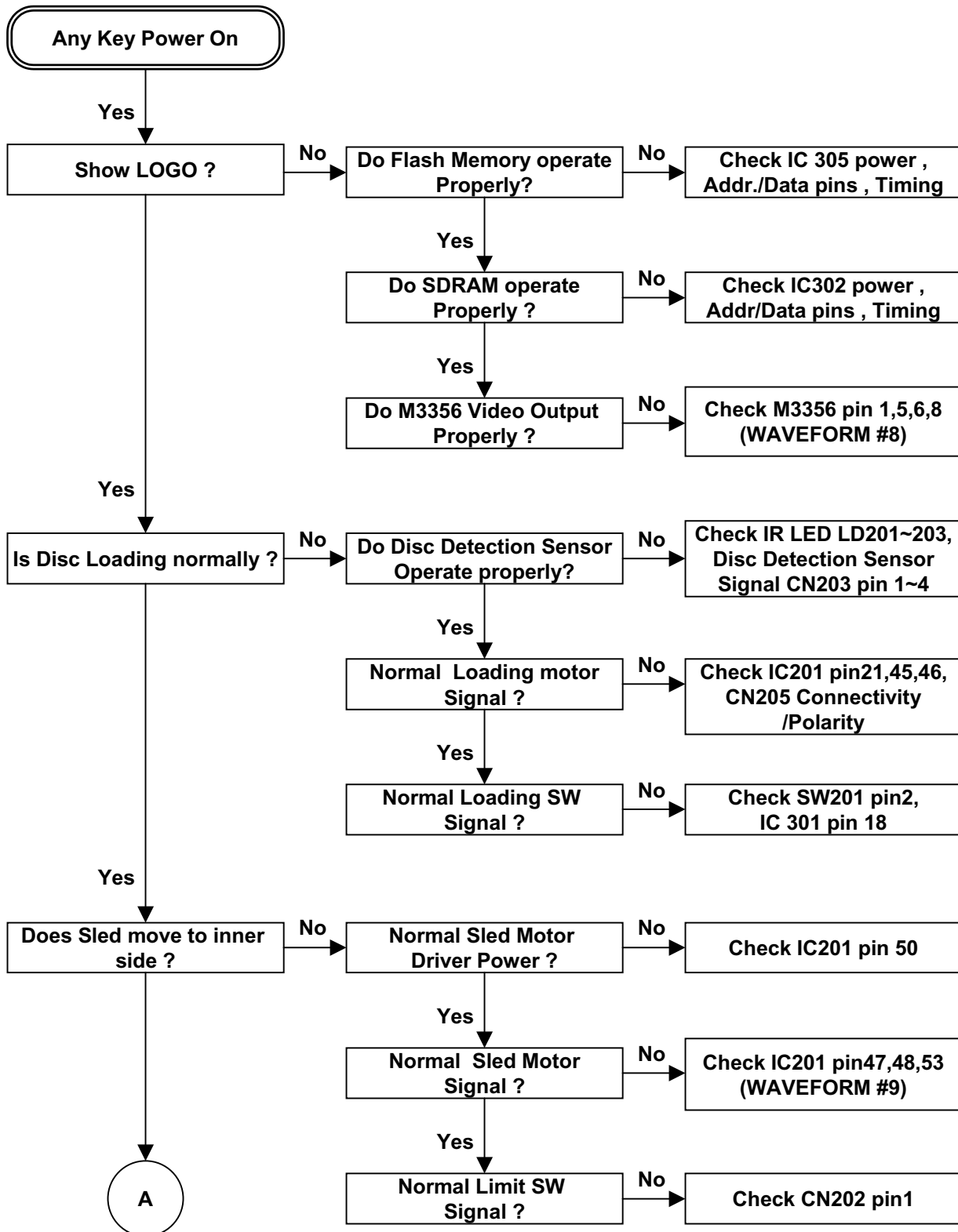
1. No Power

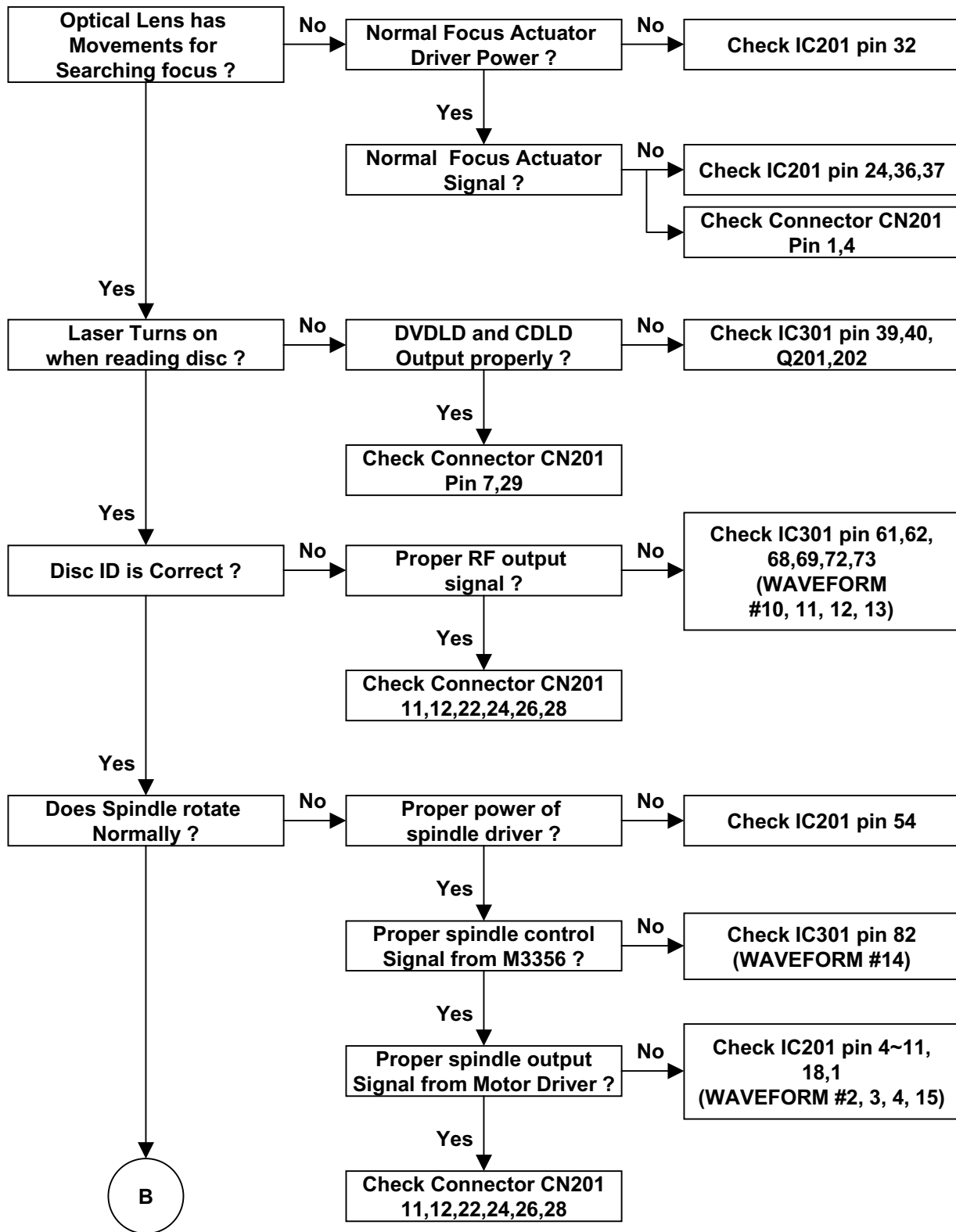


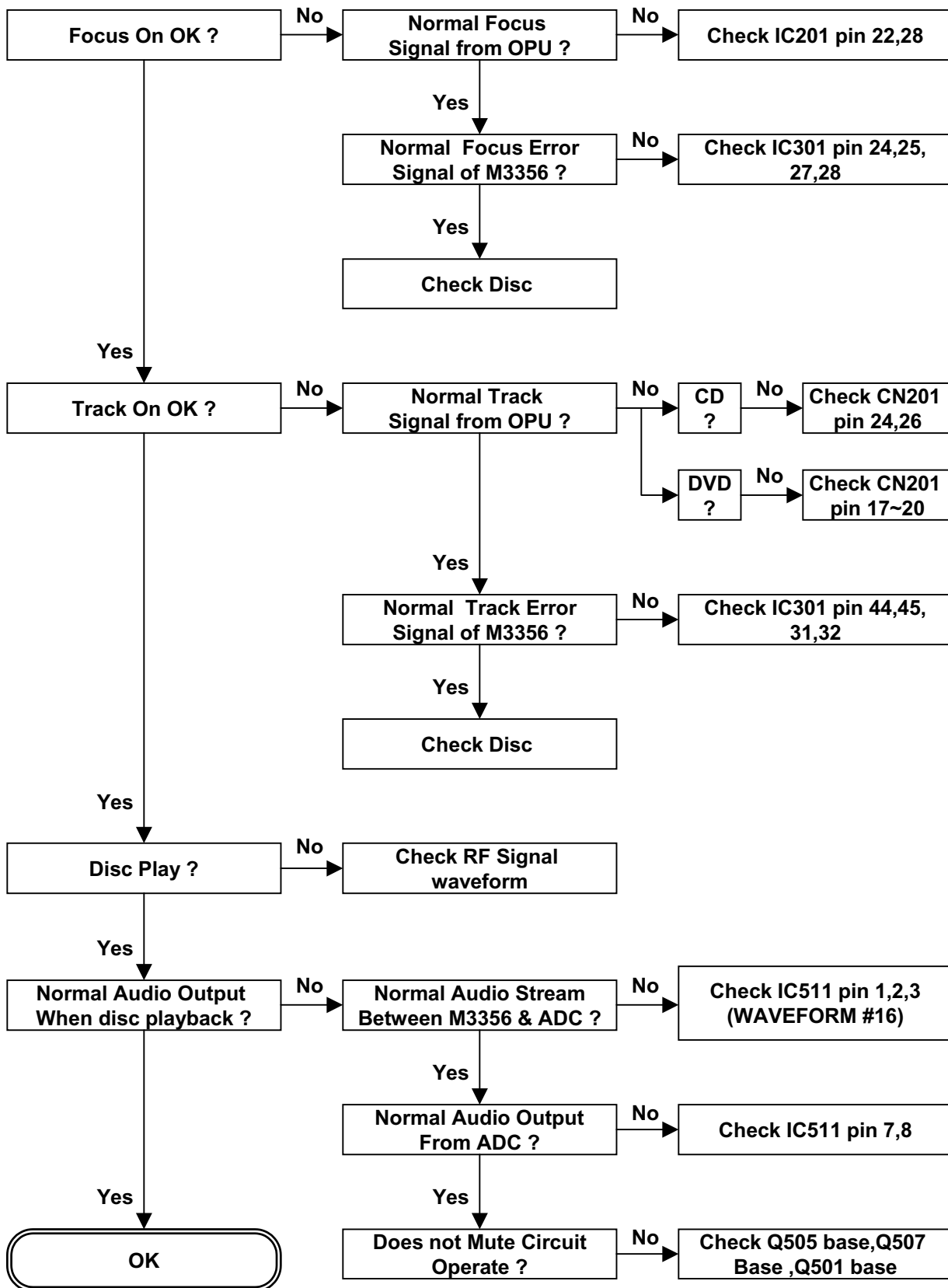
2. Front Panel Light / Display Abnormal



3. CD/DVD Part



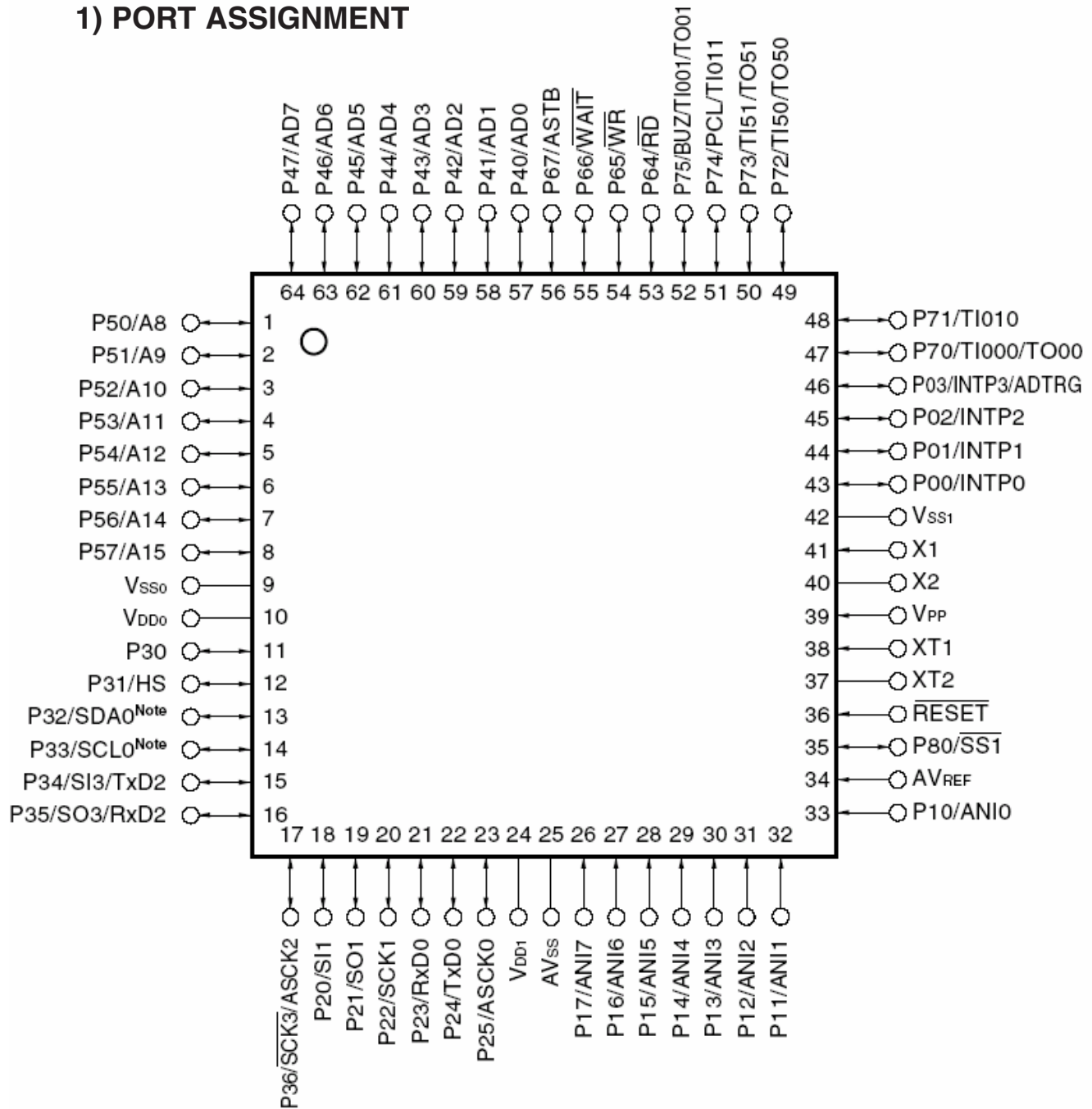




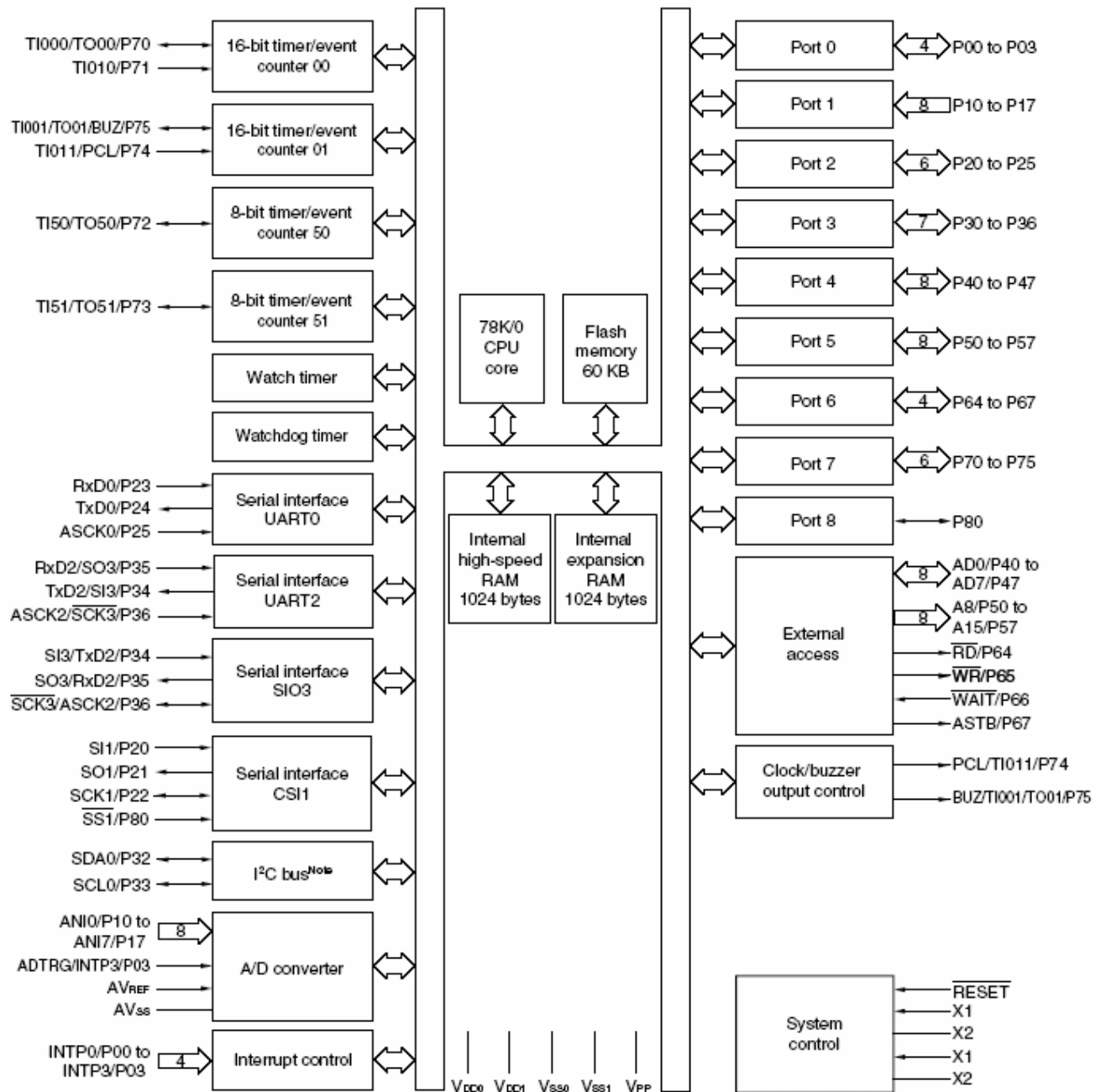
□ INTERNAL BLOCK DIAGRAM of ICs

• IC601 UPD78F0078Y

1) PORT ASSIGNMENT



2) BLOCK DIAGRAM



3) PIN FUNCTIONS

Pin Name	I/O	Function		After Reset	Alternate Function
P00	I/O	Port 0 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.		Input	INTP0
P01					INTP1
P02					INTP2
P03					INTP3/ADTRG
P10 to P17	Input	Port 1 8-bit input only port.		Input	ANI0 to ANI7
P20	I/O	Port 2 6-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.		Input	SI1
P21					SO1
P22					SCK1
P23					RxD0
P24					TxD0
P25					ASCK0
P30	I/O	Port 3 7-bit I/O port. Input/output can be specified in 1-bit units.	N-ch open-drain I/O port. LEDs can be driven directly.	Input	—
P31					HS
P32					SDA0 ^{Note}
P33					SCL0 ^{Note}
P34		Use of an on-chip pull-up resistor can be specified by a software setting.			SI3/TxD2
P35					SO3/RxD2
P36					SCK3/ASCK2
P40 to P47	I/O	Port 4 8-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting. The interrupt request flag (KRIF) is set to 1 by the falling edge detection.		Input	AD0 to AD7
P50 to P57	I/O	Port 5 8-bit I/O port. LEDs can be driven directly. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.		Input	A8 to A15
P64	I/O	Port 6 4-bit I/O port. Input/output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.		Input	$\overline{\text{RD}}$
P65					$\overline{\text{WR}}$
P66					$\overline{\text{WAIT}}$
P67					ASTB

Pin Name	I/O	Function	After Reset	Alternate Function
P70	I/O	Port 7 6-bit I/O port. Input/output can be specified 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	TI000/TO00
P71				TI010
P72				TI50/TO50
P73				TI51/TO51
P74				TI011/PCL
P75				TI001/TO01/ BUZ
P80	I/O	Port 8 1-bit I/O port. Input/output can be specified 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting.	Input	$\overline{SS1}$

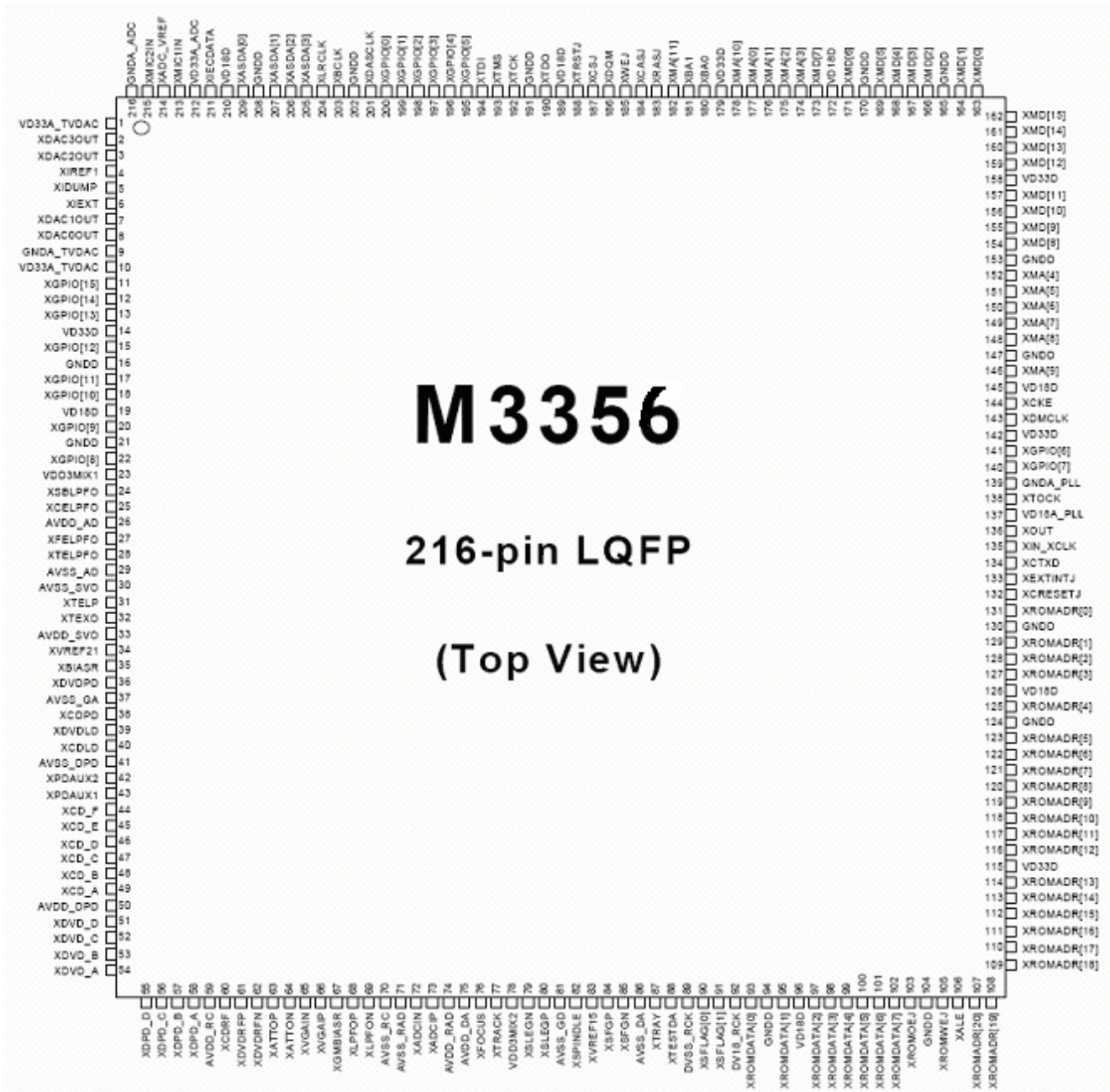
Pin Name	I/O	Function	After Reset	Alternate Function
INTP0-INTP2	Input	External interrupt request input for which the valid edge (rising edge, falling edge, or both rising edge and falling edges) can be specified.	Input	P00-P02
INTP3				P03/ADTRG
SI1	Input	Serial interface serial data input.	Input	P20
SI3				P34/TxD2
SO1	Output	Serial interface serial data output.	Input	P21
SO3				P35/RxD2
SDA0 ^{Note}	I/O	Serial interface serial data input/output.	Input	P32
SCK1	I/O	Serial interface serial clock input/output.	Input	P22
$\overline{SCK3}$				P36/ASCK2
SCL0 ^{Note}				P33
$\overline{SS1}$	Input	Serial interface chip select input.	Input	P80
RxD0	Input	Serial data input for asynchronous serial interface.	Input	P23
RxD2				P35/SO3
TxD0	Output	Serial data output for asynchronous serial interface.	Input	P24
TxD2				P34/SI3
ASCK0	Input	Serial clock input for asynchronous serial interface.	Input	P25
ASCK2				P36/ $\overline{SCK3}$
TI000	Input	External count clock input to 16-bit timer/event counter 00. Capture trigger input to capture register 000, 010 of 16-bit timer/event counter 00.	Input	P70/TO00
TI010		Capture trigger input to capture register 000 of 16-bit timer/event counter 00.		P71
TI001		External count clock input to 16-bit timer/event counter 01. Capture trigger input to capture register 001, 011 of 16-bit timer/event counter 01.		P75/TO01/ BUZ
TI011		Capture trigger input to capture register 001 of 16-bit timer/event counter 01.		P74/PCL
TI50		External count clock input to 8-bit timer/event counter 50.		P72/TO50
TI51		External count clock input to 8-bit timer/event counter 51.		P73/TO51

Pin Name	I/O	Function	After Reset	Alternate Function
TO00	Output	16-bit timer/event counter 00 output.	Input	P70/TI000
TO01		16-bit timer/event counter 01 output.		P75/TI001/ BUZ
TO50		8-bit timer/event counter 50 output.		P72/TI50
TO51		8-bit timer/event counter 51 output.		P73/TI51
PCL	Output	Clock output (for trimming of main system clock and subsystem clock).	Input	P74/TI011
BUZ	Output	Buzzer output.	Input	P75/TI001/ TO01
AD0 to AD7	I/O	Lower address/data bus for extending memory externally.	Input	P40 to P47
A8 to A15	Output	Higher address bus for extending memory externally.	Input	P50 to P57
$\overline{\text{RD}}$	Output	Strobe signal output for read operation of external memory.	Input	P64
$\overline{\text{WR}}$		Strobe signal output for write operation of external memory.		P65
$\overline{\text{WAIT}}$	Input	Inserting wait for accessing external memory.	Input	P66
ASTB	Output	Strobe output which externally latches address information output to port 4 and port 5 to access external memory.	Input	P67
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
ADTRG	Input	A/D converter trigger signal input.	Input	P03/INTP3
HS	Output	Handshake output when writing data to the flash memory using SIO3.	Input	P31
AVREF	Input	A/D converter reference voltage and analog power supply.	—	—
AVSS	—	A/D converter ground potential. Set the same potential as that of VSS0 or VSS1.	—	—
X1	Input	Connecting crystal resonator for main system clock oscillation.	—	—
X2	—		—	—
XT1	Input	Connecting crystal resonator for subsystem clock oscillation.	—	—
XT2	—		—	—
$\overline{\text{RESET}}$	Input	System reset input.	Input	—
VDD0	—	Positive power supply for ports.	—	—
VDD1	—	Positive power supply (except ports).	—	—
VSS0	—	Ground potential of ports.	—	—
VSS1	—	Ground potential (except ports).	—	—
VPP	—	Applying high-voltage for program write/verify. Connect directly to VSS0 or VSS1 in normal operation mode.	—	—

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0-P02/INTP2	8-C	I/O	Input: Independently connect to V_{SS0} via a resistor.
P03/INTP3/ADTRG			Output: Leave open.
P10/ANI0 to P17/ANI7	25	Input	Connect to V_{DD0} or V_{SS0} .
P20/SI1	8-C	I/O	Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P21/SO1	5-H		
P22/SCK1	8-C		
P23/RxD0	5-H		
P24/TxD0			
P25/ASCK0	8-C		
P30	13-P		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P31/HS			
P32, P33 (μ PD78F0078 only)			
P32/SDA0 (μ PD78F0078Y only)	13-R		Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P33/SCL0 (μ PD78F0078Y only)			
P34/SI3/TxD2	8-C		
P35/SO3/RxD2			
P36/SCK3/ASCK2			
P40/AD0 to P47/AD7	5-H		Input: Independently connect to V_{DD0} via a resistor. Output: Leave open.
P50/A8 to P57/A15			
P64/ $\overline{RD}$			Input: Independently connect to V_{DD0} or V_{SS0} via a resistor. Output: Leave open.
P65/ $\overline{WR}$			
P66/ $\overline{WAIT}$			
P67/ASTB			
P70/TI000/TO00	8-C		Input: Connect to V_{SS0} via a resistor. Output: Leave open.
P71/TI010			
P72/TI50/TO50			
P73/TI51/TO51			
P74/TI011/PCL			
P75/TI001/TO01/BUZ			
P80/ $\overline{SS1}$			
$\overline{RESET}$	2	Input	—
XT1	16	—	Connect to V_{DD0} .
XT2			Leave open.
AV_{REF}	—		Connect to V_{SS0} .
AV_{SS}			Connect directly to V_{SS0} or V_{SS1} .
V_{PP}			

• IC301 M3356

1) PORT ASSIGNMENT

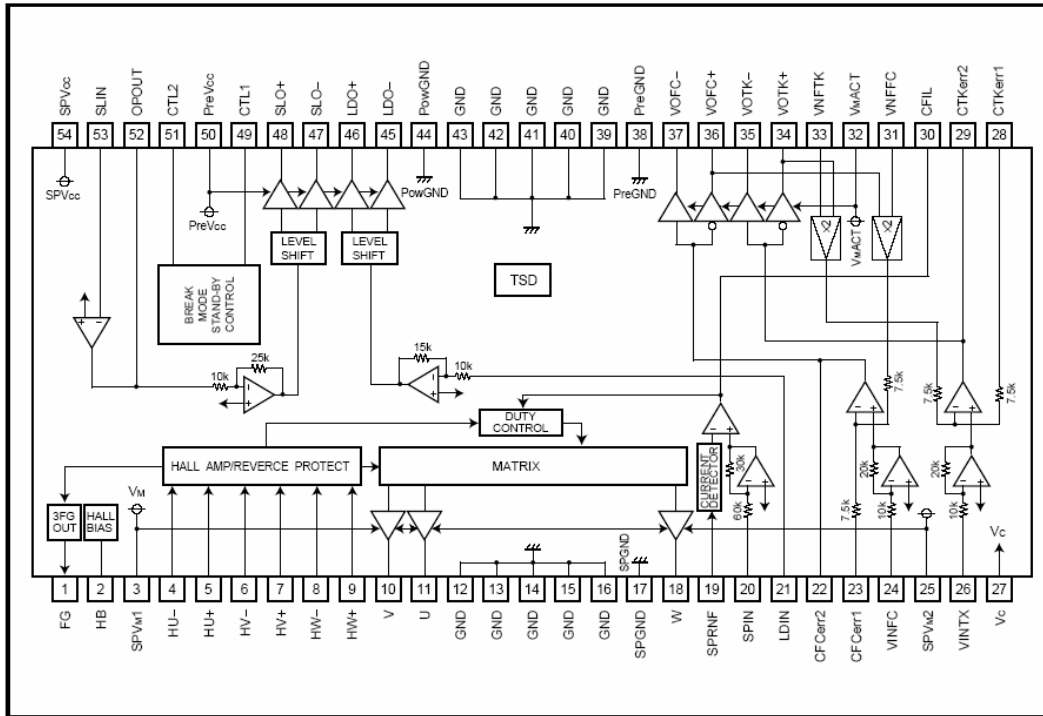


2) PIN DESCRIPTION

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VD33A_TVDAC	55	XDPD_D	109	XROMADR[18]	163	XMD[0]
2	XDAC3OUT	56	XDPD_C	110	XROMADR[17]	164	XMD[1]
3	XDAC2OUT	57	XDPD_B	111	XROMADR[16]	165	GNDD
4	XIREF1	58	XDPD_A	112	XROMADR[15]	166	XMD[2]
5	XIDUMP	59	AVDD_RC	113	XROMADR[14]	167	XMD[3]
6	XIEXT	60	XCDRF	114	XROMADR[13]	168	XMD[4]
7	XDAC1OUT	61	XDVDRFP	115	VD33D	169	XMD[5]
8	XDAC0OUT	62	XDVDRFN	116	XROMADR[12]	170	GNDD
9	GNDA_TVDAC	63	XATTOP	117	XROMADR[11]	171	XMD[6]
10	VD33A_TVDAC	64	XATTON	118	XROMADR[10]	172	VD18D
11	XGPIO[15]	65	XVGAIN	119	XROMADR[9]	173	XMD[7]
12	XGPIO[14]	66	XVGAIP	120	XROMADR[8]	174	XMA[3]
13	XGPIO[13]	67	XGMBIASR	121	XROMADR[7]	175	XMA[2]
14	VD33D	68	XLFPFOP	122	XROMADR[6]	176	XMA[1]
15	XGPIO[12]	69	XLPFON	123	XROMADR[5]	177	XMA[0]
16	GNDD	70	AVSS_RC	124	GNDD	178	XMA[10]
17	XGPIO[11]	71	AVSS_RAD	125	XROMADR[4]	179	VD33D
18	XGPIO[10]	72	XADCIN	126	VD18D	180	XBA0
19	VD18D	73	XADCIP	127	XROMADR[3]	181	XBA1
20	XGPIO[9]	74	AVDD_RAD	128	XROMADR[2]	182	XMA[11]
21	GNDD	75	AVDD_DA	129	XROMADR[1]	183	XRASJ
22	XGPIO[8]	76	XFOCUS	130	GNDD	184	XCASJ
23	VDD3MIX1	77	XTRACK	131	XROMADR[0]	185	XWEJ
24	XSBLPFO	78	VDD3MIX2	132	XCRESETJ	186	XDQM
25	XCELPFO	79	XSLEGN	133	XEXTINTJ	187	XCSJ
26	AVDD_AD	80	XSLEGP	134	XCTXD	188	XTRSTJ
27	XFELPFO	81	AVSS_GD	135	XIN_XCLK	189	VD18D
28	XTELPFO	82	XSPINDLE	136	XOUT	190	XTDO
29	AVSS_AD	83	XVREF15	137	VD18A_PLL	191	GNDD
30	AVSS_SVO	84	XSFGP	138	XTOCK	192	XTCK
31	XTELP	85	XSFGN	139	GNDA_PLL	193	XTMS
32	XTEXO	86	AVSS_DA	140	XGPIO[7]	194	XTDI
33	AVDD_SVO	87	XTRAY	141	XGPIO[6]	195	XGPIO[5]
34	XVREF21	88	XTESTDA	142	VD33D	196	XGPIO[4]
35	XBIASR	89	DVSS_RCK	143	XDMCLK	197	XGPIO[3]
36	XDVDPD	90	XSFLAG[0]	144	XCKE	198	XGPIO[2]
37	AVSS_GA	91	XSFLAG[1]	145	VD18D	199	XGPIO[1]
38	XCDPD	92	DV18_RCK	146	XMA[9]	200	XGPIO[0]
39	XDVDLD	93	XROMDATA[0]	147	GNDD	201	XDASCLK
40	XCDLD	94	GNDD	148	XMA[8]	202	GNDD
41	AVSS_DPD	95	XROMDATA[1]	149	XMA[7]	203	XBCLK
42	XPDAUX2	96	VD18D	150	XMA[6]	204	XLRCLK
43	XPDAUX1	97	XROMDATA[2]	151	XMA[5]	205	XASDA[3]
44	XCD_F	98	XROMDATA[3]	152	XMA[4]	206	XASDA[2]
45	XCD_E	99	XROMDATA[4]	153	GNDD	207	XASDA[1]
46	XCD_D	100	XROMDATA[5]	154	XMD[8]	208	GNDD
47	XCD_C	101	XROMDATA[6]	155	XMD[9]	209	XASDA[0]
48	XCD_B	102	XROMDATA[7]	156	XMD[10]	210	VD18D
49	XCD_A	103	XROMOEJ	157	XMD[11]	211	XIECDATA
50	AVDD_DPD	104	GNDD	158	VD33D	212	VD33A_ADC
51	XDVD_D	105	XROMWEJ	159	XMD[12]	213	XMIC1IN
52	XDVD_C	106	XALE	160	XMD[13]	214	XADC_VREF
53	XDVD_B	107	XROMADR[20]	161	XMD[14]	215	XMIC2IN
54	XDVD_A	108	XROMADR[19]	162	XMD[15]	216	GNDA_ADC

• IC201 BD7903FS

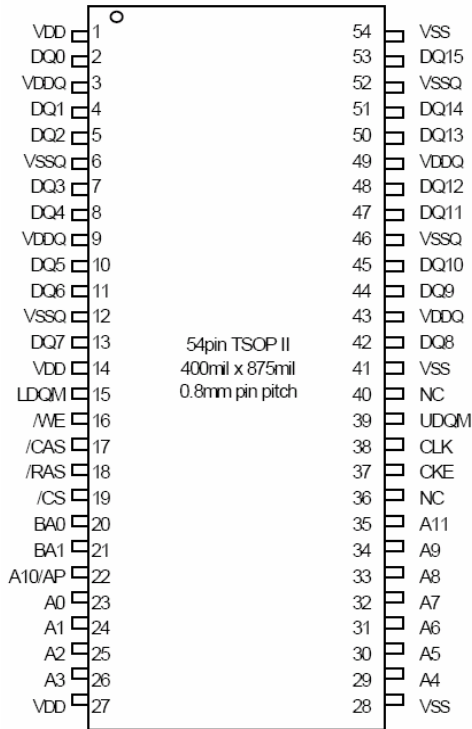
1) PORT ASSIGNMENT & BLOCK DIAGRAM



Pin No.	Pin name	Function
1	FG	Frequency generator output
2	HB	Hall bias
3	SPVM1	Spindle driver power supply 1
4	HU-	Hall amp.U negative input
5	HU+	Hall amp.U positive input
6	HV-	Hall amp.V negative input
7	HV+	Hall amp.V positive input
8	HW-	Hall amp.W negative input
9	HW+	Hall amp.W positive input
10	V	Spindle driver output V
11	U	Spindle driver output U
12	GND	GND
13	GND	GND
14	GND	GND
15	GND	GND
16	GND	GND
17	SPGND	Spindle driver power ground
18	W	Spindle driver output W
19	SPRNF	Spindle driver current sense
20	SPIN	Spindle driver input
21	LDIN	Loading driver input
22	CFCerr2	Connection with capacitor for error amplifier
23	CFCerr1	Connection with capacitor for error amplifier
24	VINFC	Focus driver input
25	SPVM2	Spindle driver power supply 2
26	VINTK	Tracking driver input
27	Vc	Reference voltage input

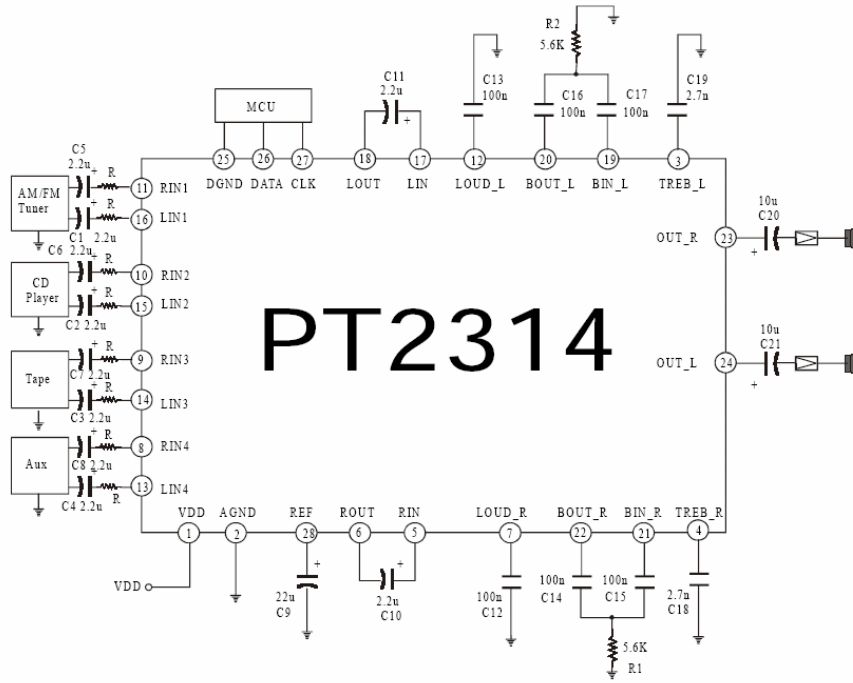
Pin No.	Pin name	Function
28	CTKerr1	Connection with capacitor for error amplifier
29	CTKerr2	Connection with capacitor for error amplifier
30	CFIL	Connection with capacitor for spindle loop
31	VNFFC	Feedback for focus driver
32	VMACT	Actuator driver block power supply
33	VNFTK	Feedback for tracking driver
34	VOTK+	Tracking driver positive output
35	VOTK-	Tracking driver negative output
36	VOFC+	Focus driver positive output
37	VOFC-	Focus driver negative output
38	PreGND	Pre-ground
39	GND	GND
40	GND	GND
41	GND	GND
42	GND	GND
43	GND	GND
44	PowGND	BTL block power ground
45	LDO-	Loading driver negative output
46	LDO+	Loading driver positive output
47	SLO1-	Slide drive negative output
48	SLO1+	Slide drive positive output
49	CTL1	Driver logic control input 1
50	PreVcc	Loading block power supply
51	CTL2	Driver logic control input 2
52	OPOUT	OP amp output
53	SLIN	Slide driver input
54	SPVcc	Spindle block control power supply

• **C302 HY57V641620HG**
1) PORT ASSIGNMENT

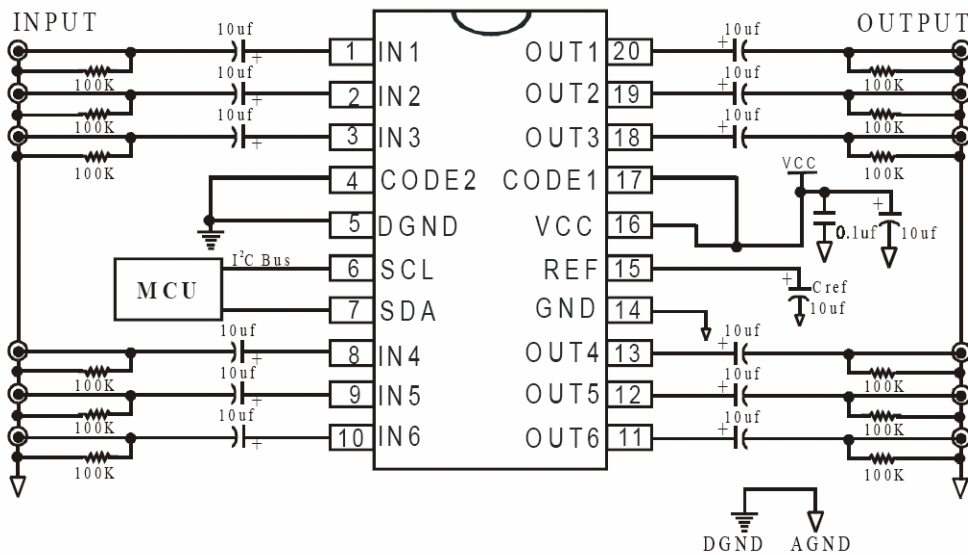


PIN	PIN NAME	DESCRIPTION
CLK	Clock	The system clock input. All other inputs are registered to the SDRAM on the rising edge of CLK
CKE	Clock Enable	Controls internal clock signal and when deactivated, the SDRAM will be one of the states among power down, suspend or self refresh
$\overline{CS}$	Chip Select	Enables or disables all inputs except CLK, CKE and DQM
BA0,BA1	Bank Address	Selects bank to be activated during $\overline{RAS}$ activity Selects bank to be read/written during $\overline{CAS}$ activity
A0 ~ A11	Address	Row Address : RA0 ~ RA11, Column Address : CA0 ~ CA7 Auto-precharge flag : A10
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Row Address Strobe, Column Address Strobe, Write Enable	$\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation Refer function truth table for details
LDQM, UDQM	Data Input/Output Mask	Controls output buffers in read mode and masks input data in write mode
DQ0 ~ DQ15	Data Input/Output	Multiplexed data input / output pin
Vdd/Vss	Power Supply/Ground	Power supply for internal circuits and input buffers
VDDQ/VSSQ	Data Output Power/Ground	Power supply for output buffers
NC	No Connection	No connection

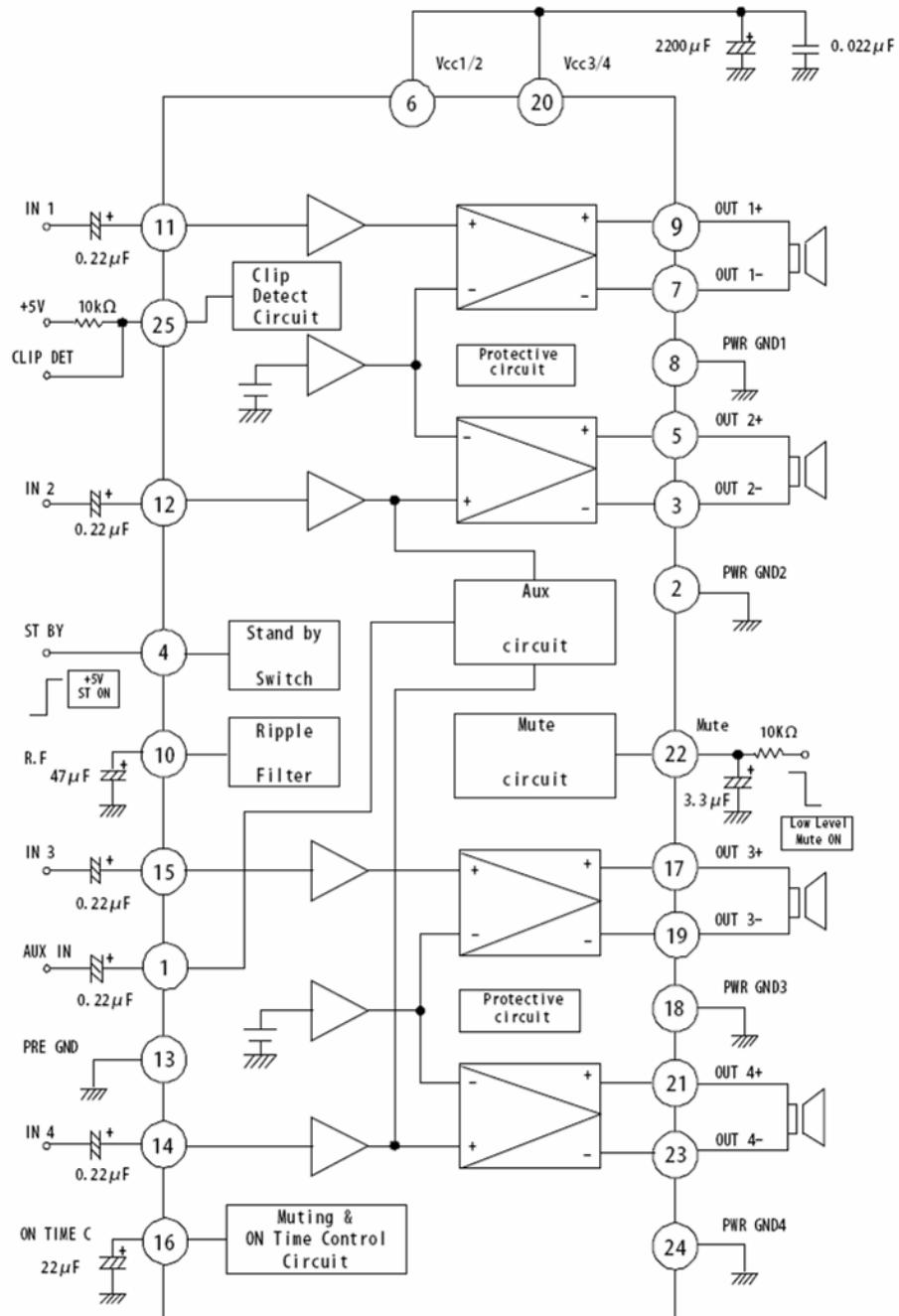
- **IC501 PT2314**
PORT ASSIGNMENT



- **IC506 PT2258**
PORT ASSIGNMENT

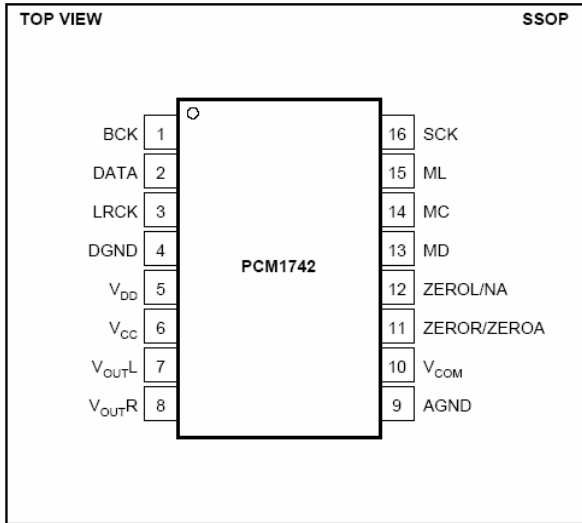


- **IC508 LA47532**
PORT ASSIGNMENT



• IC511 PCM1742

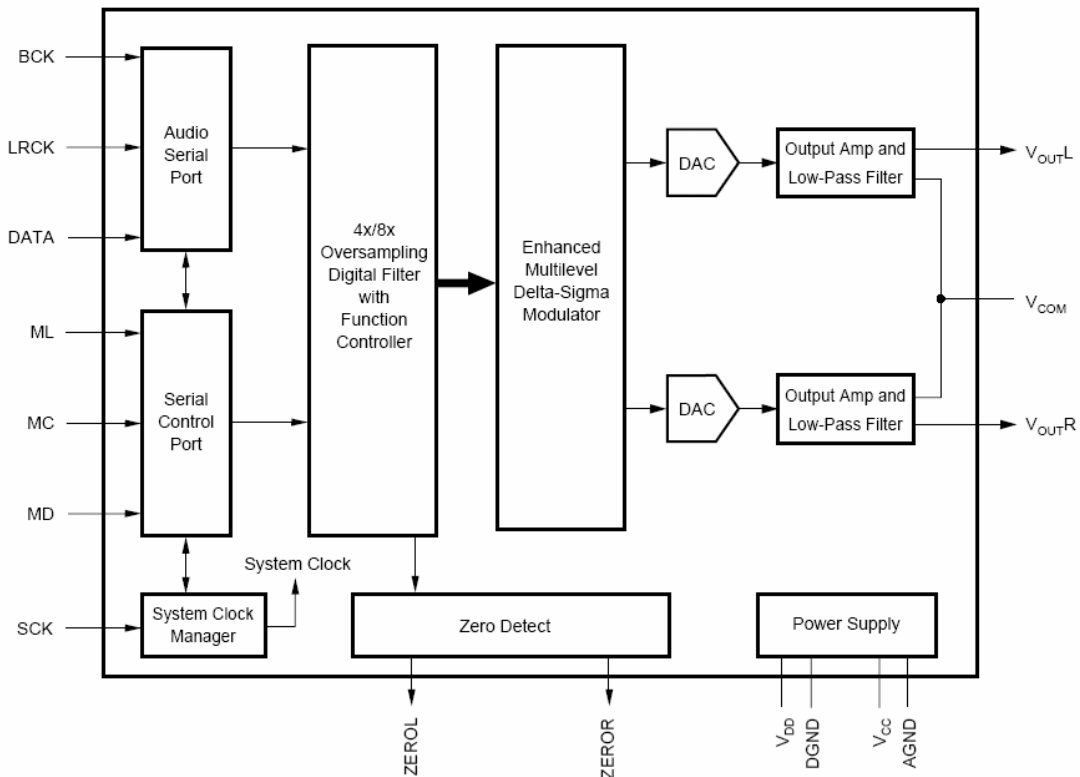
1) PORT ASSIGNMENT



PIN	NAME	TYPE	FUNCTION
1	BCK	IN	Audio Data Bit Clock Input. ⁽¹⁾
2	DATA	IN	Audio Data Digital Input. ⁽¹⁾
3	LRCK	IN	L-Channel and R-Channel Audio Data Latch Enable Input. ⁽¹⁾
4	DGND	–	Digital Ground
5	V _{DD}	–	Digital Power Supply, +3.3V
6	V _{CC}	–	Analog Power Supply, +5V
7	V _{OUTL}	OUT	Analog Output for L-Channel.
8	V _{OUTR}	OUT	Analog Output for R-Channel.
9	AGND	–	Analog Ground
10	V _{COM}	–	Common Voltage Decoupling.
11	ZEROR/ZEROA	OUT	Zero Flag Output for R-Channel/Zero Flag Output for L/R-Channel.
12	ZEROL/NA	OUT	Zero Flag Output for L-Channel/No Assign.
13	MD	IN	Mode Control Data Input. ⁽²⁾
14	MC	IN	Mode Control Clock Input. ⁽²⁾
15	ML	IN	Mode Control Latch Input. ⁽²⁾
16	SCK	IN	System Clock Input.

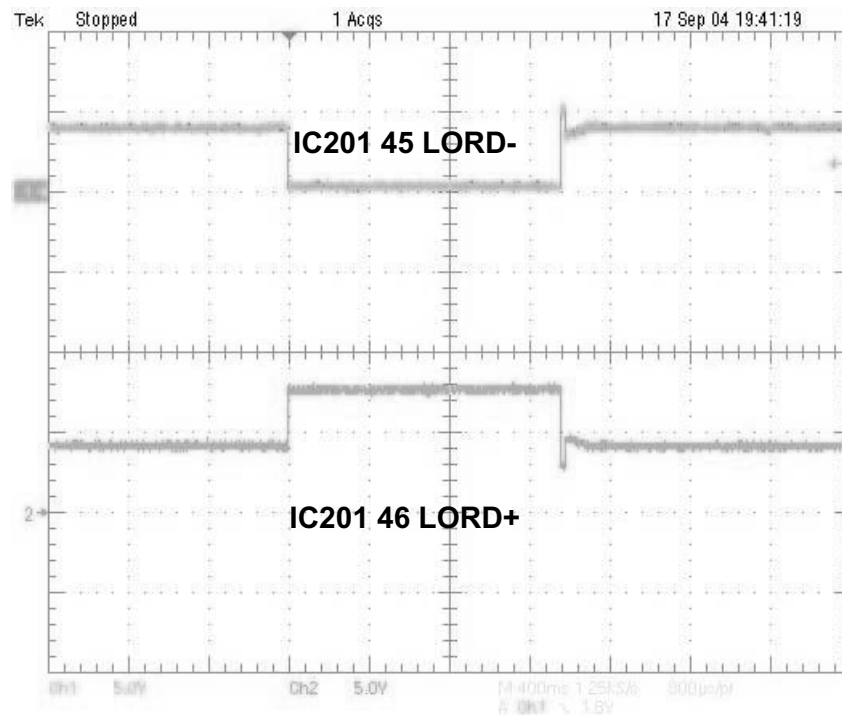
NOTES: (1) Schmitt-trigger input, 5V tolerant. (2) Schmitt-trigger with internal pull-down, 5V tolerant.

2) BLOCK DIAGRAM

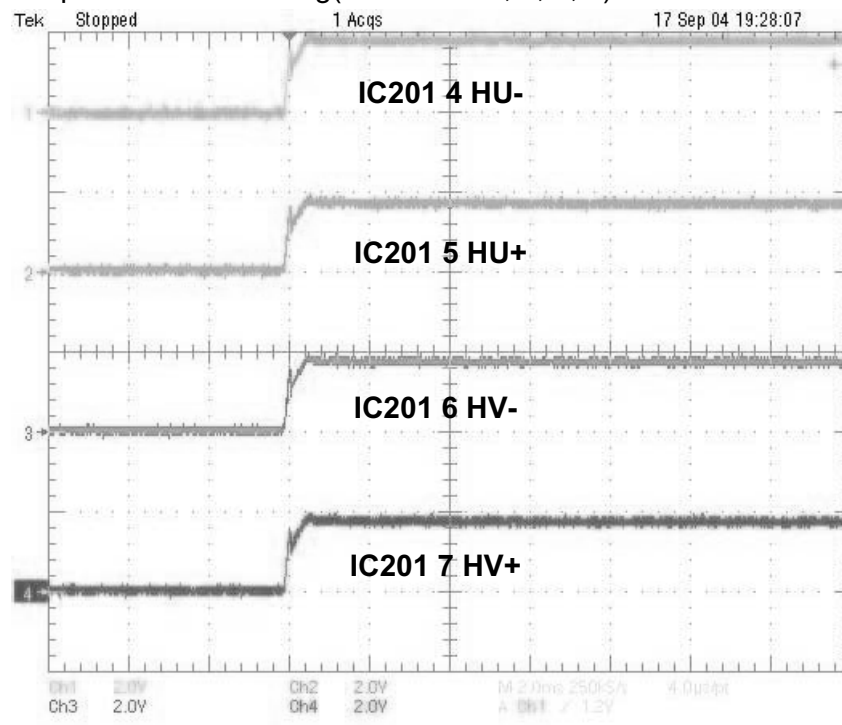


❑ DETAILS AND WAVEFORMS ON SYSTEM TEST AND DEBUGGING

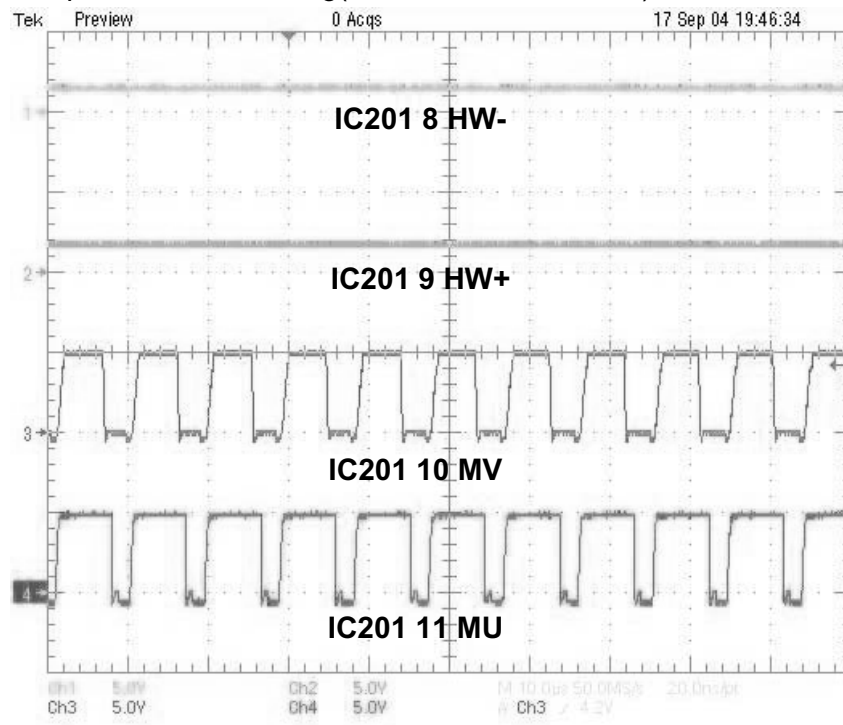
#1. Disc Lording(IC201 PIN 45,46)



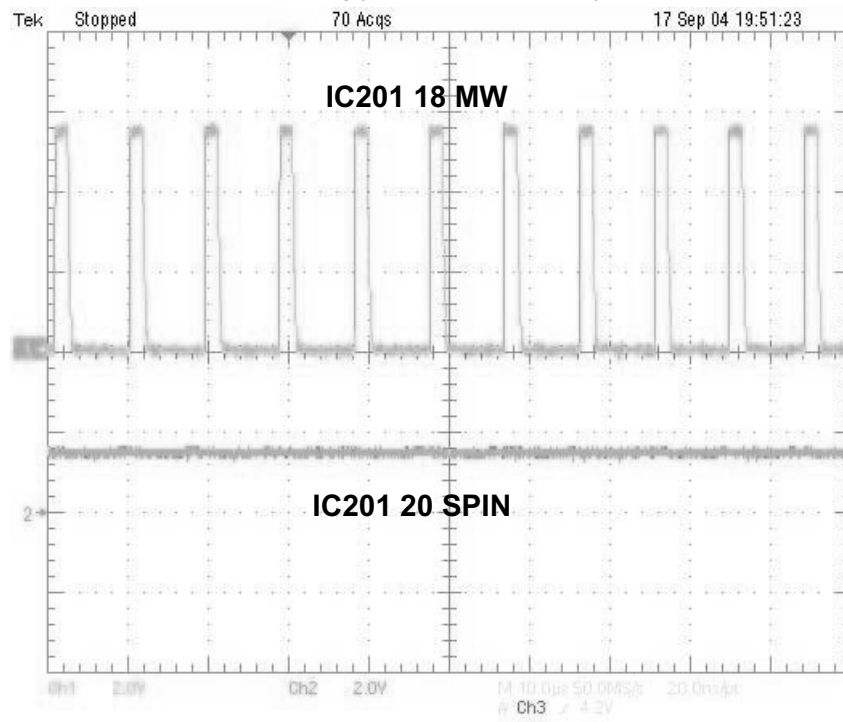
#2. Spindle motor rotating(IC201 PIN 4, 5, 6, 7)



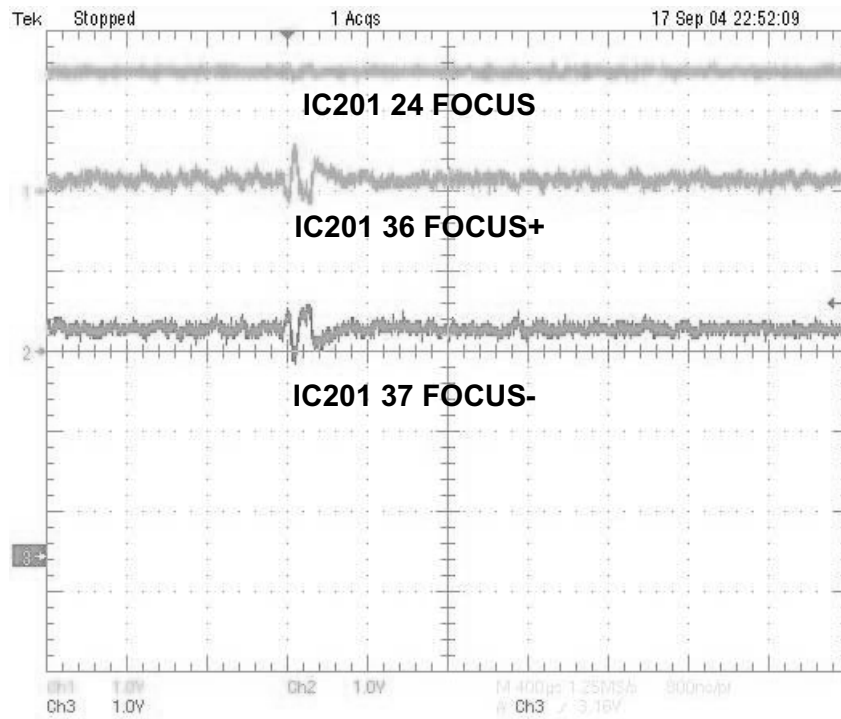
#3. Spindle motor rotating(IC201 PIN 8, 9, 10, 11)



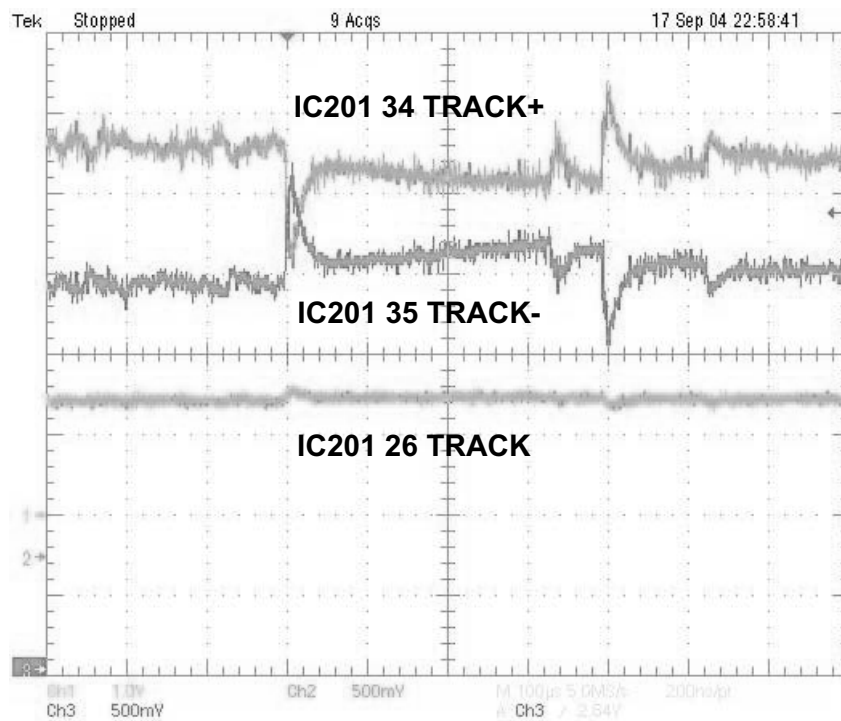
#4. Spindle motor rotating(IC201 PIN 18, 20)



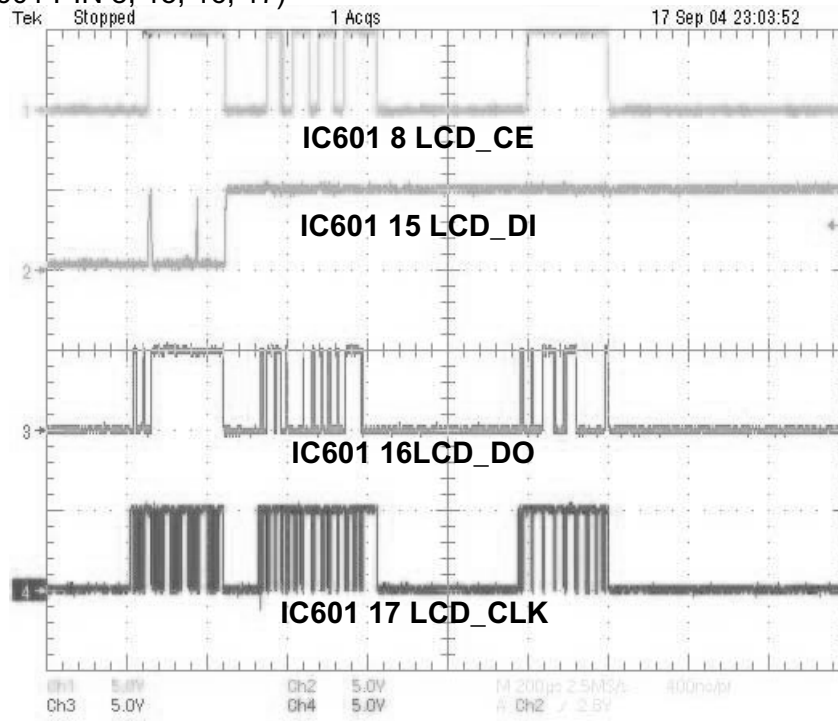
#5. focus control signal(IC201 PIN 24, 36, 37)



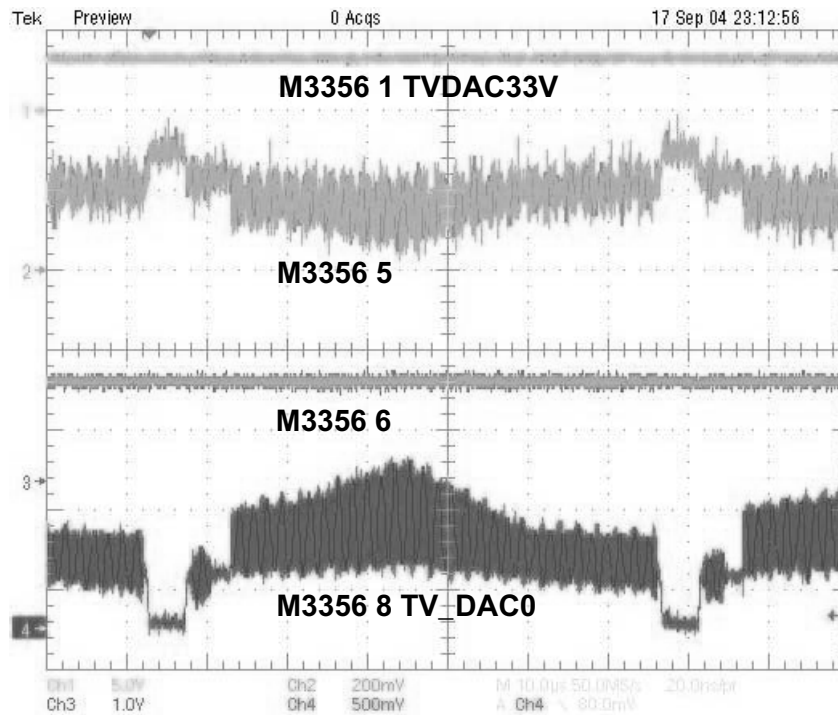
#6. tracking control signal(IC201 PIN 26, 34, 35)



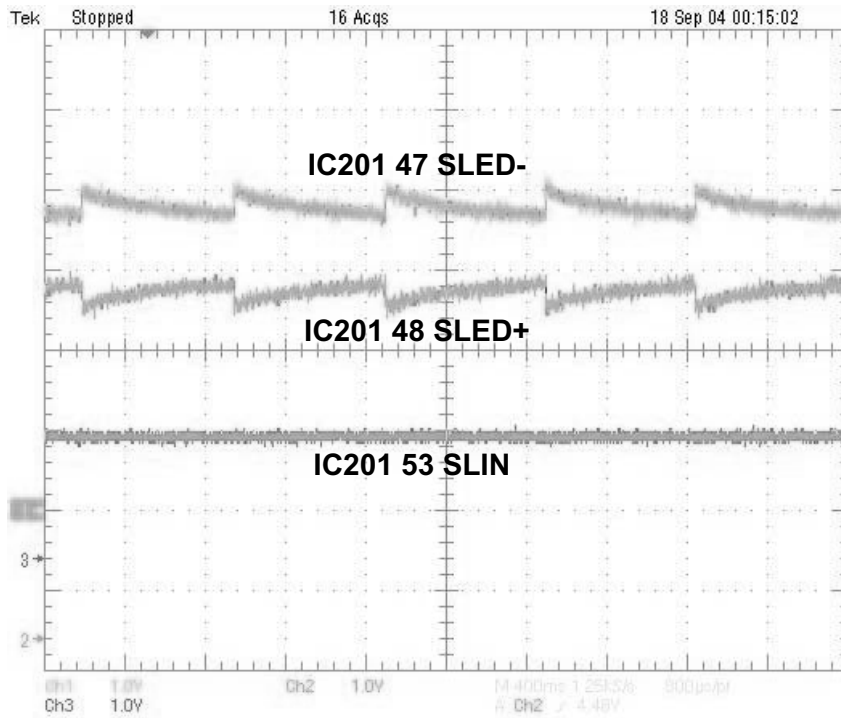
#7. Communication signal between Micom and Front Panel
(IC601 PIN 8, 15, 16, 17)



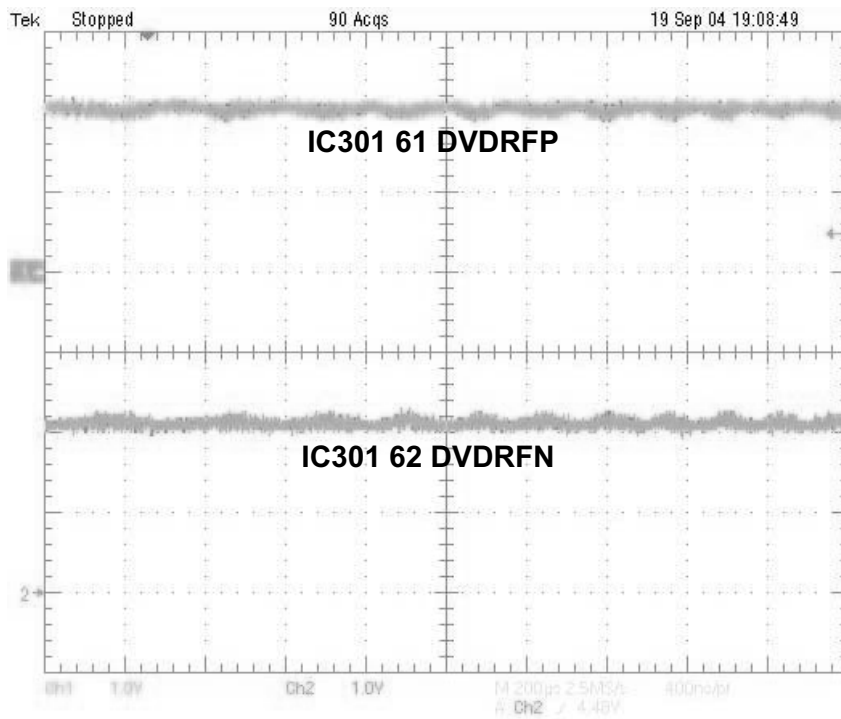
#8. Normal Video Output(M3356 PIN 1, 5, 6, 8)



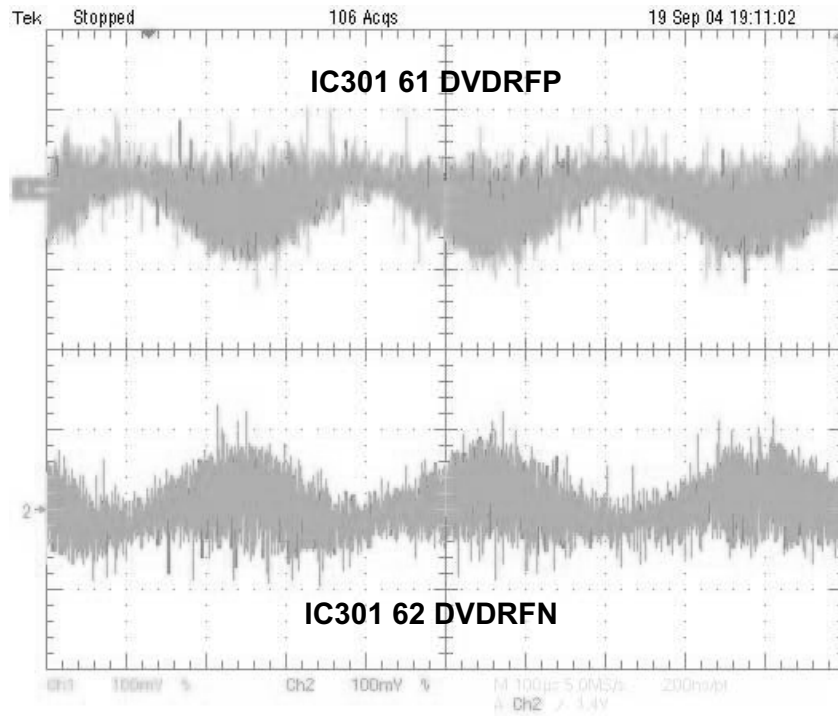
#9. Sled Motor control signal(IC201 PIN 47, 48, 53)



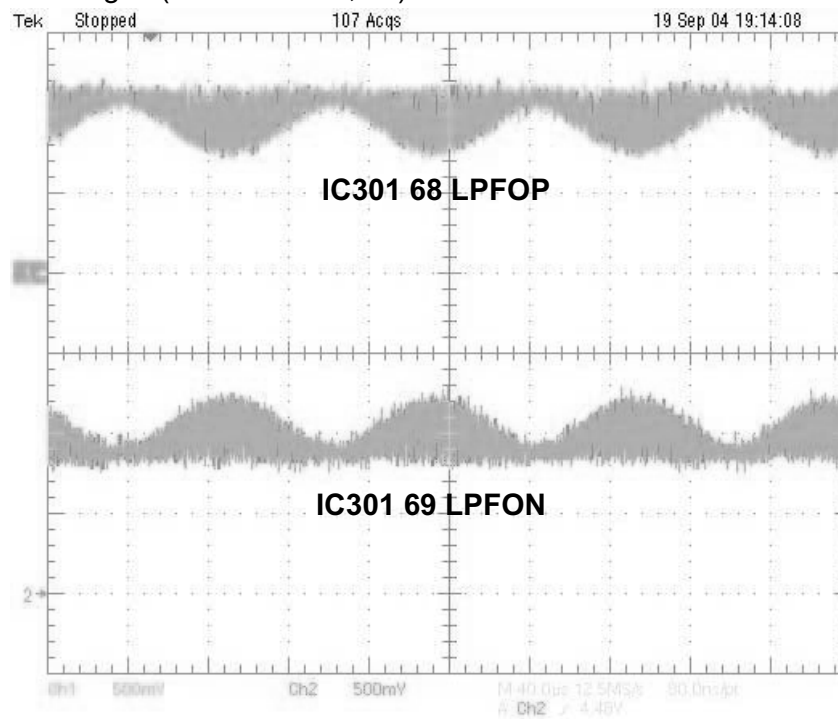
#10. RF signal(IC301 PIN 61, 62)



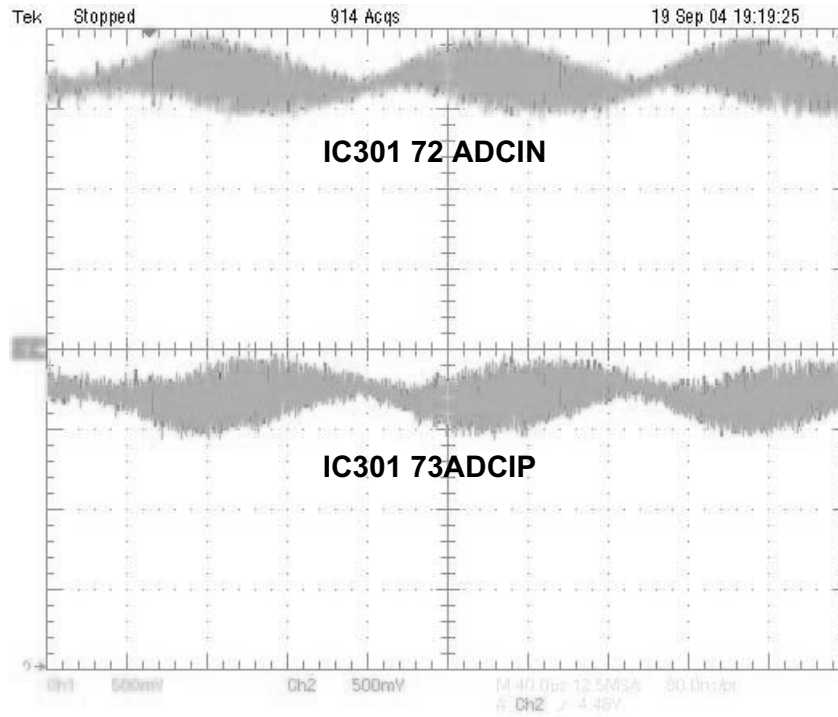
#11. RF signal(IC301 PIN 61, 62)



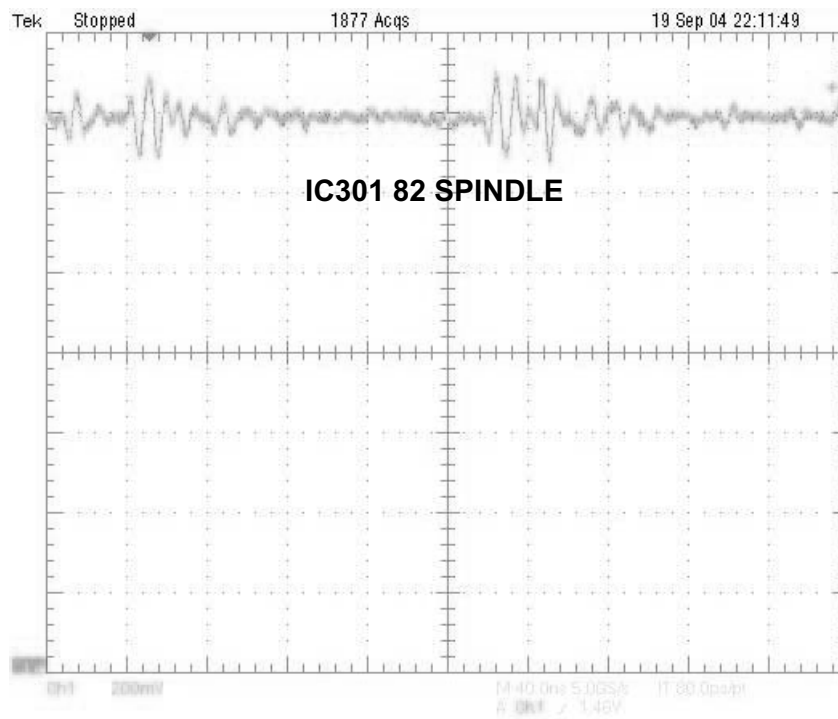
#12. RF signal(IC301 PIN 68, 69)



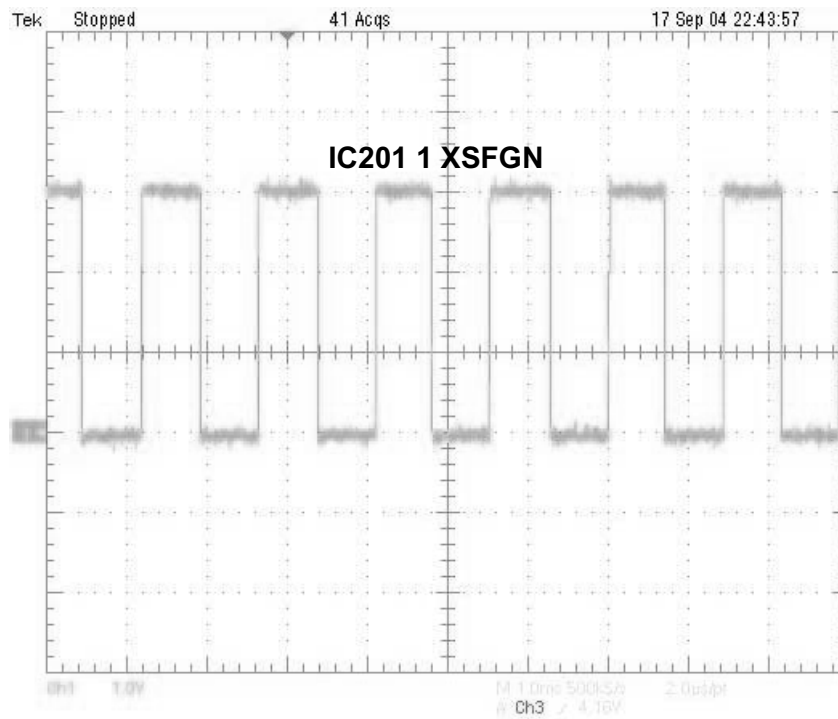
#13. RF signal(IC301 PIN 72, 73)



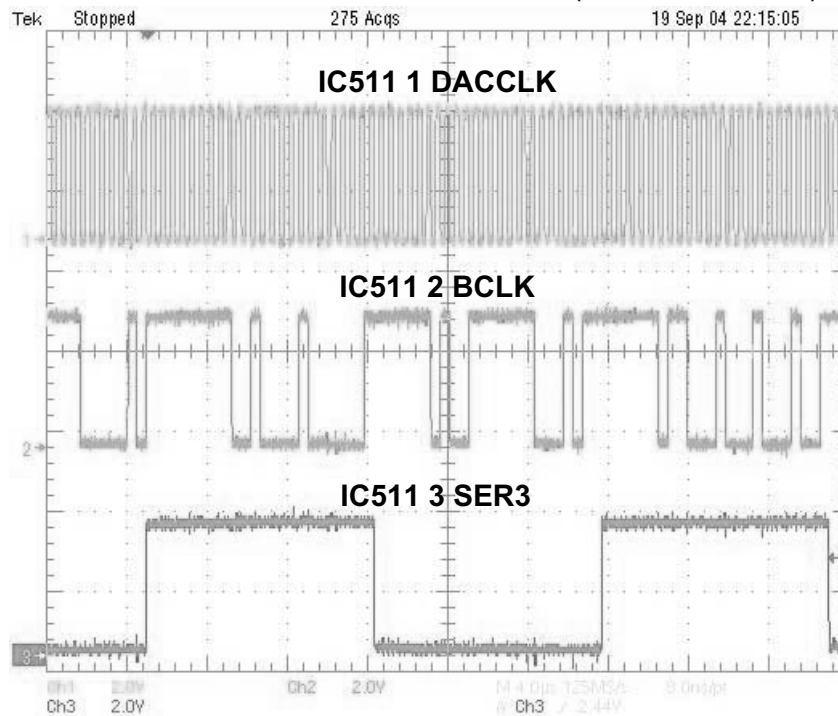
#14. Spindle control signal(IC301 PIN 82)



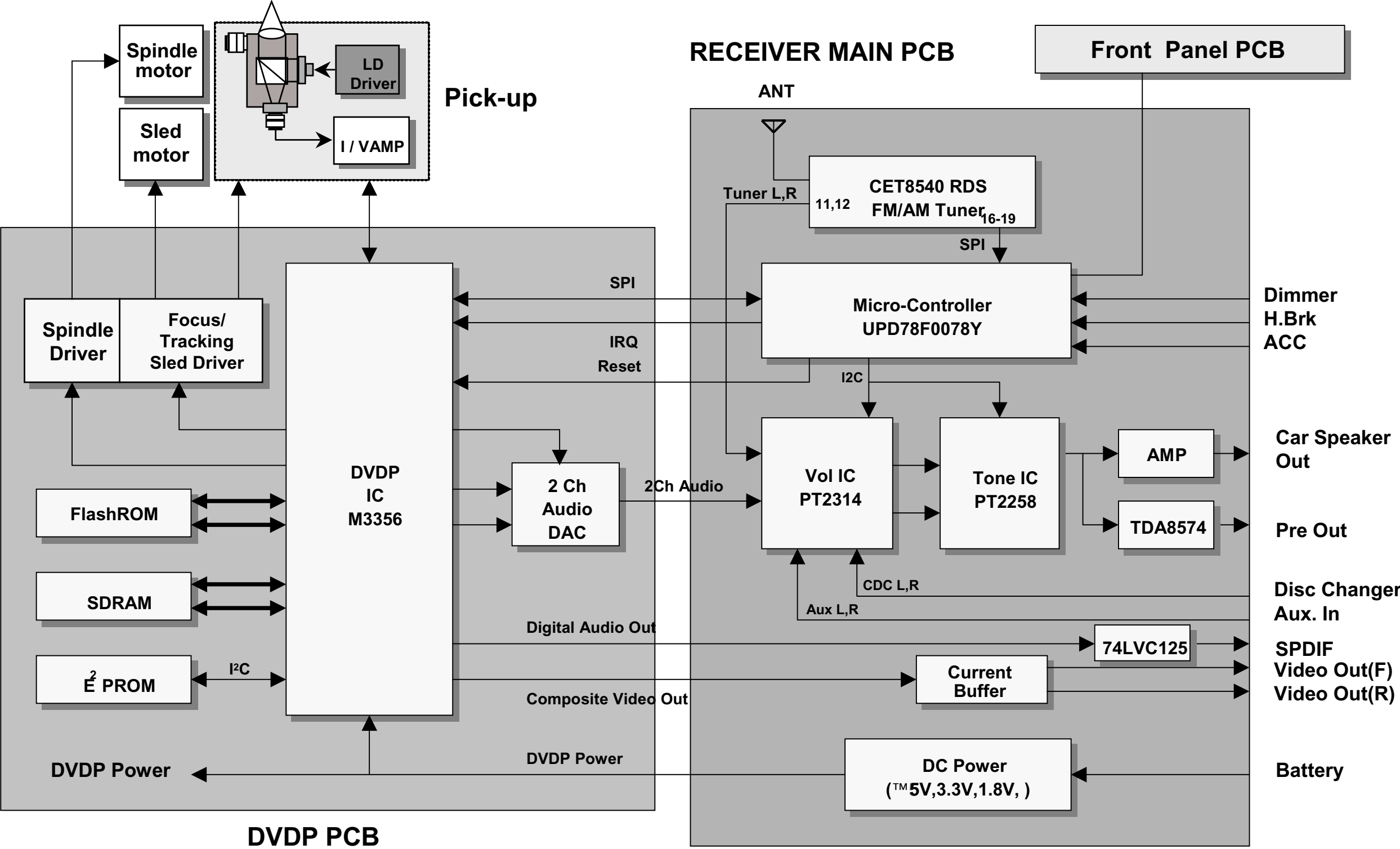
#15. Spindle output signal(IC201 PIN 1)



#16. Audio Stream between M3356 and ADC (IC511 PIN 1, 2, 3)

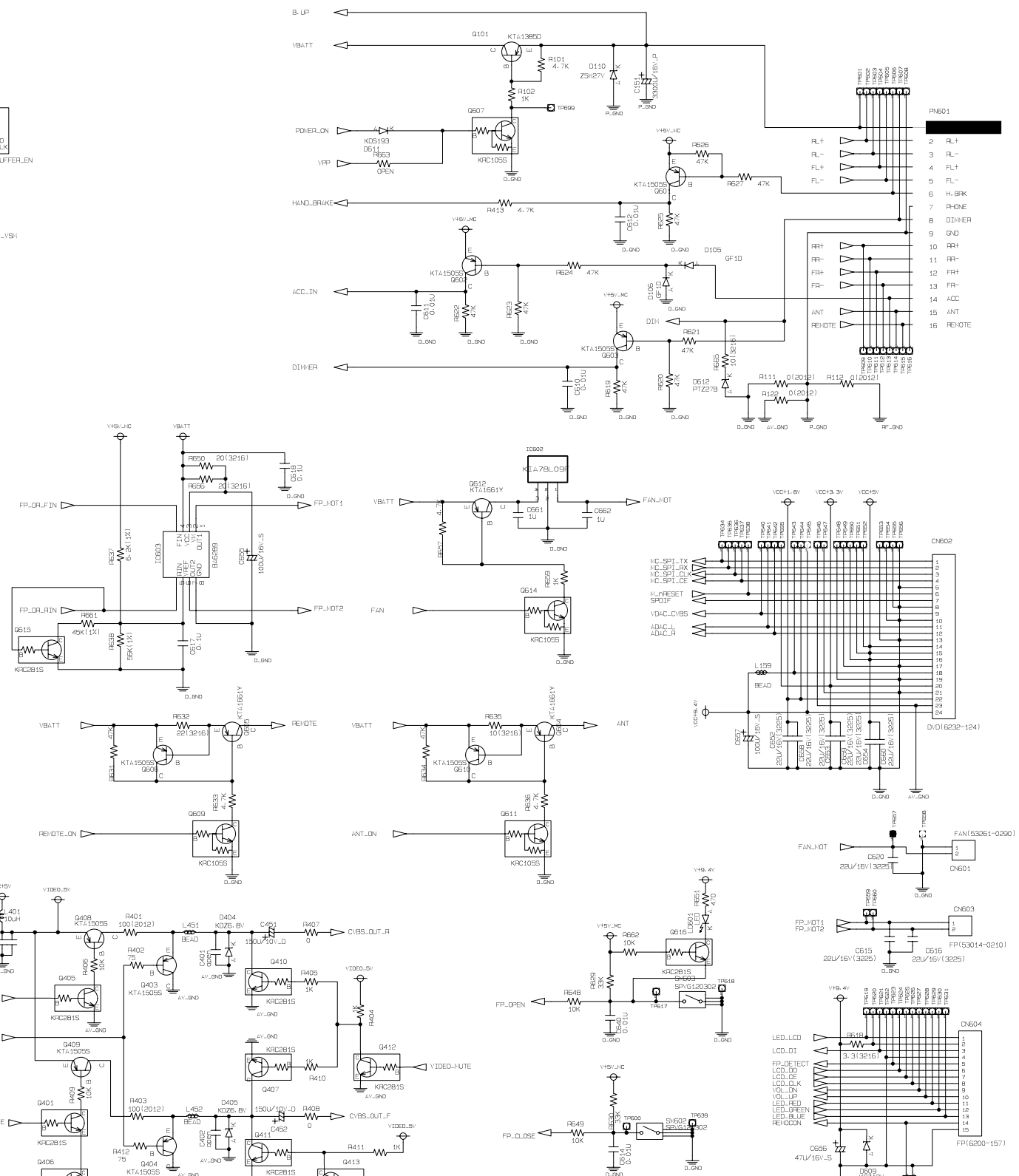
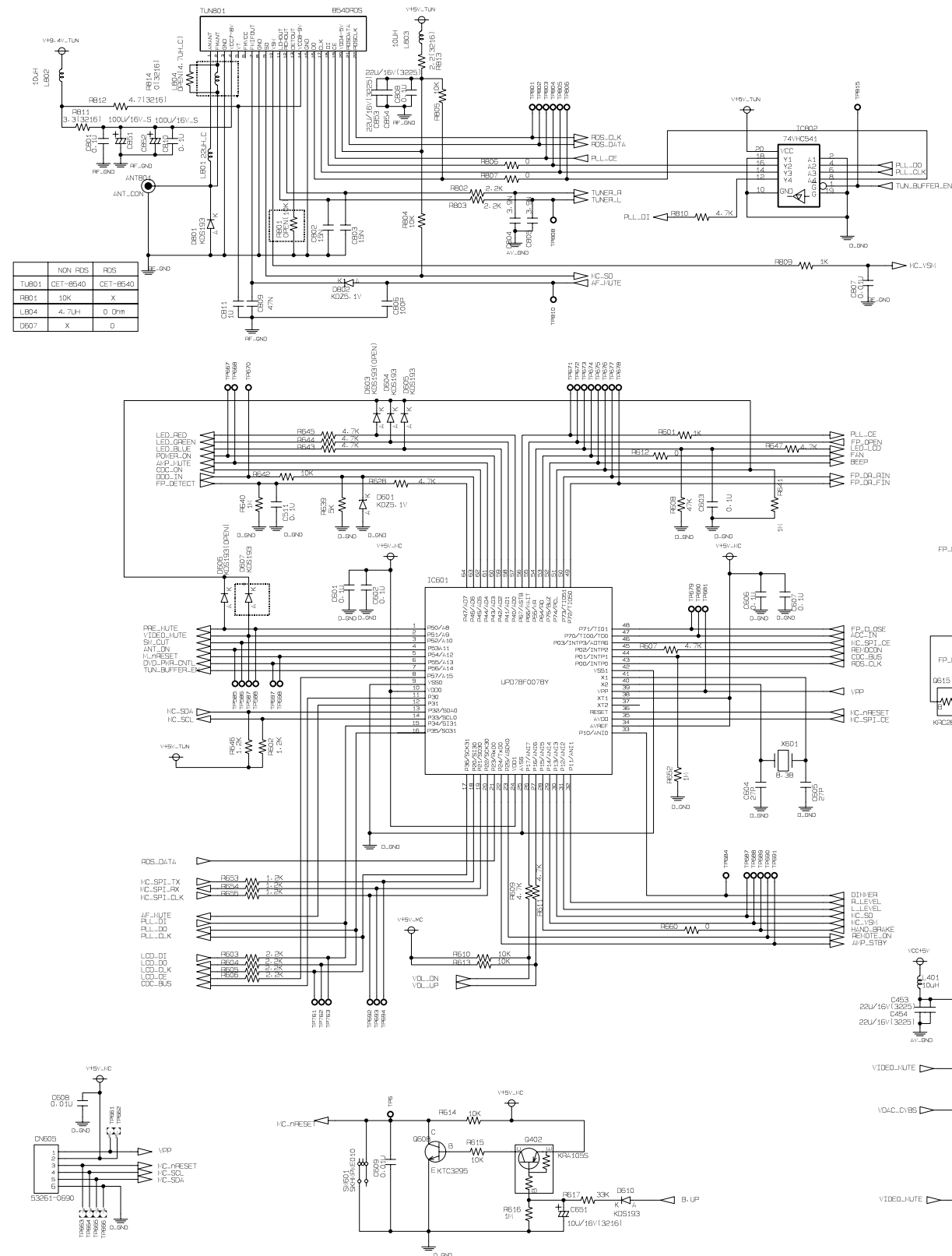


❑ BLOCK DIAGRAM

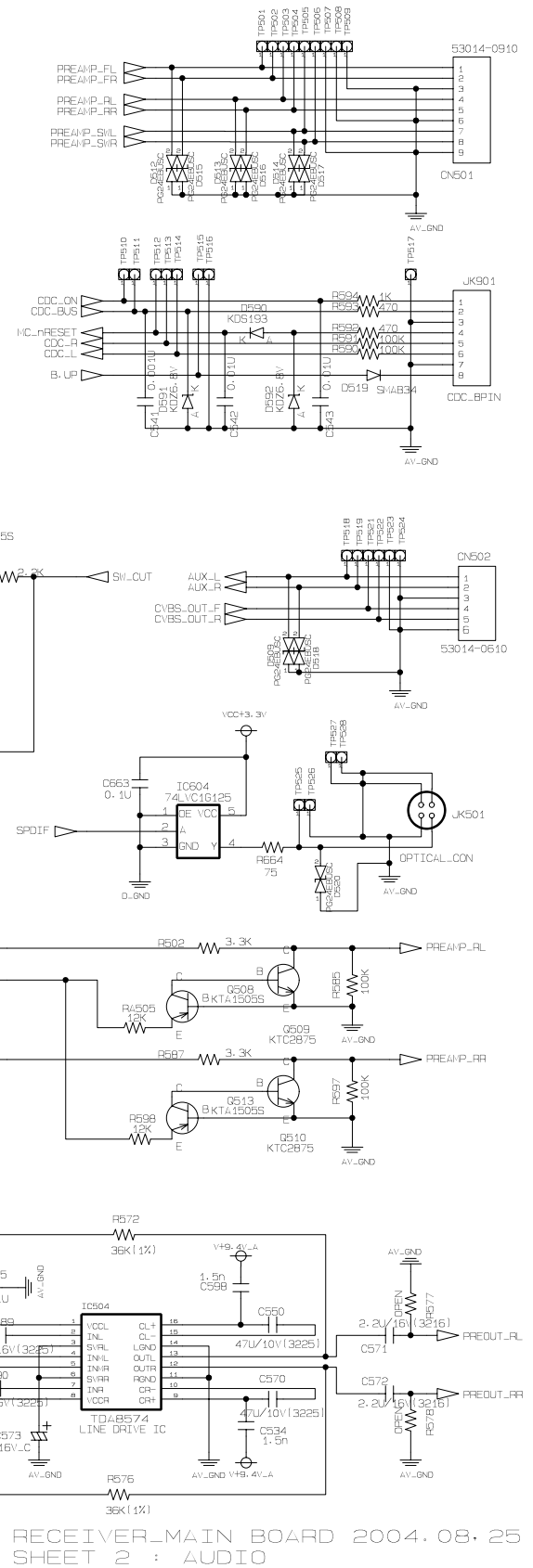
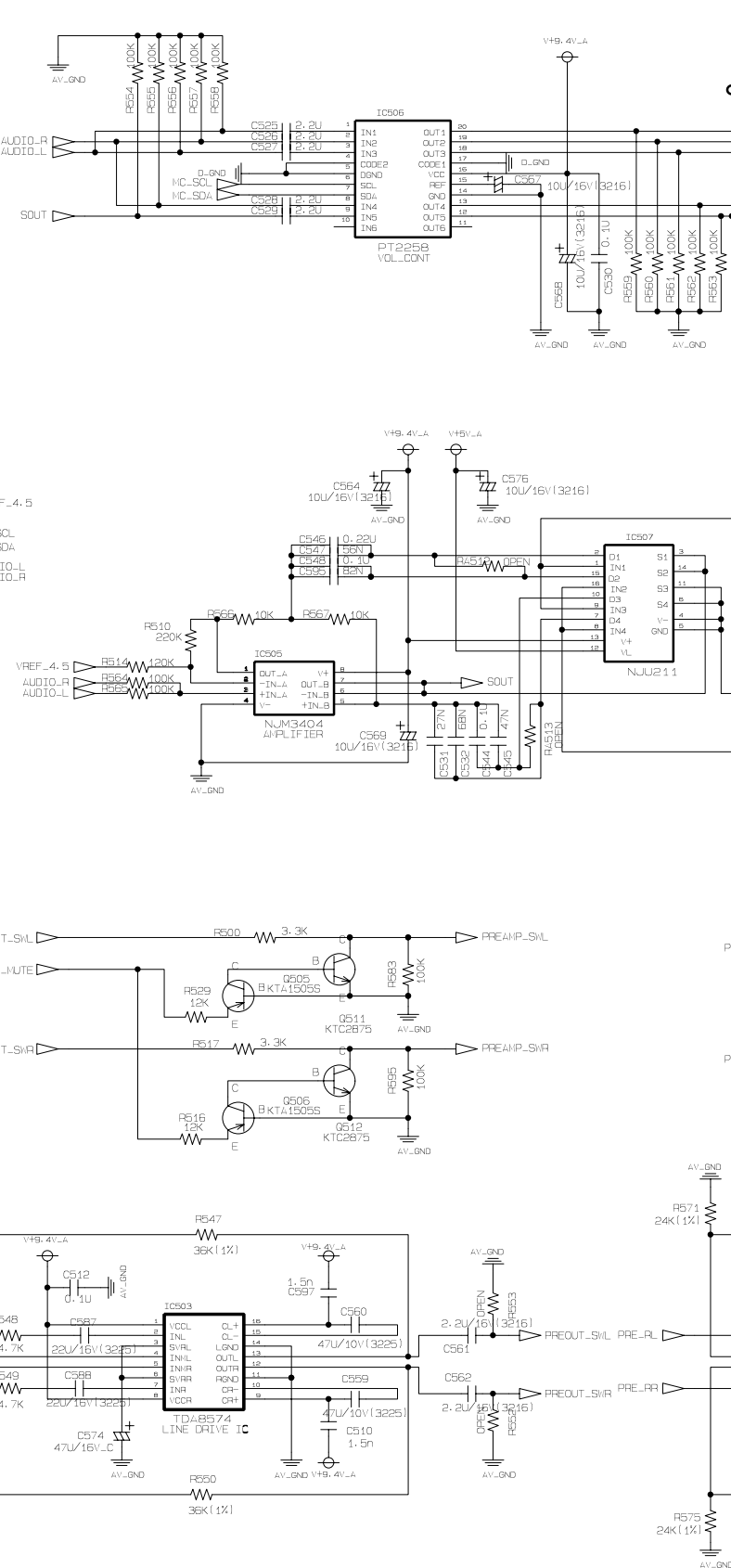
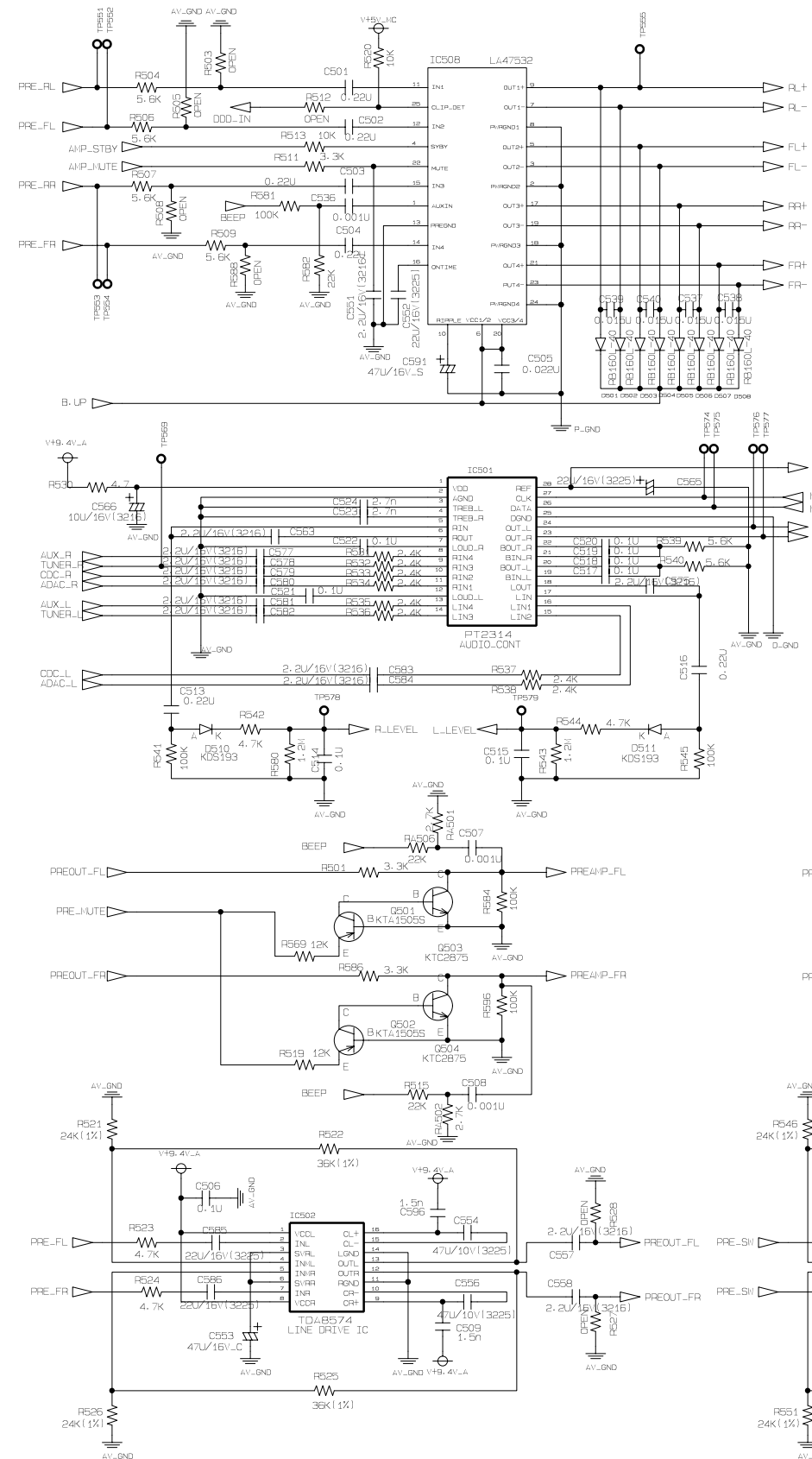


SCHEMATIC DIAGRAMS

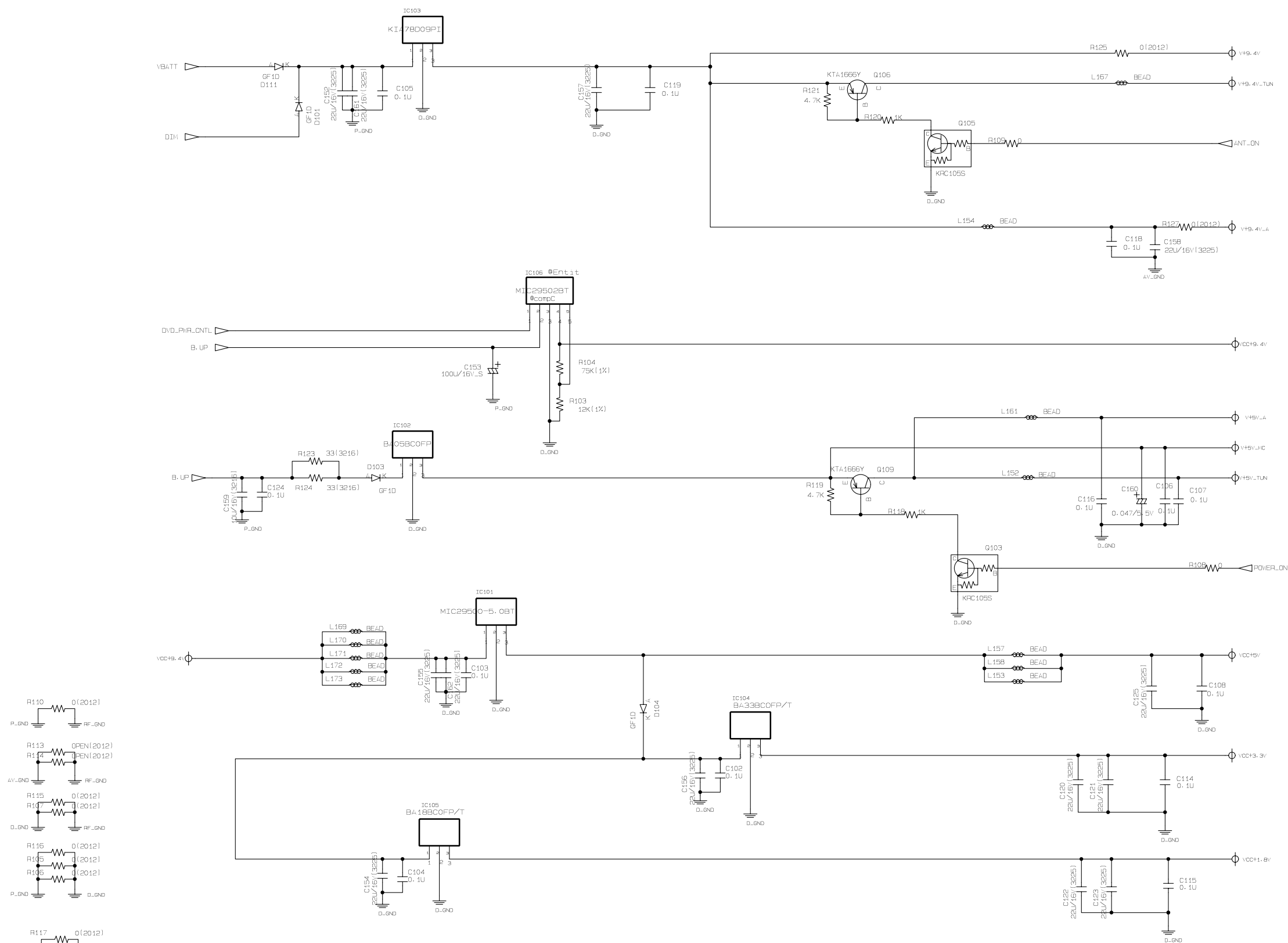
MICOM SCHEMATIC DIAGRAM



- **AUDIO SCHEMATIC DIAGRAM**

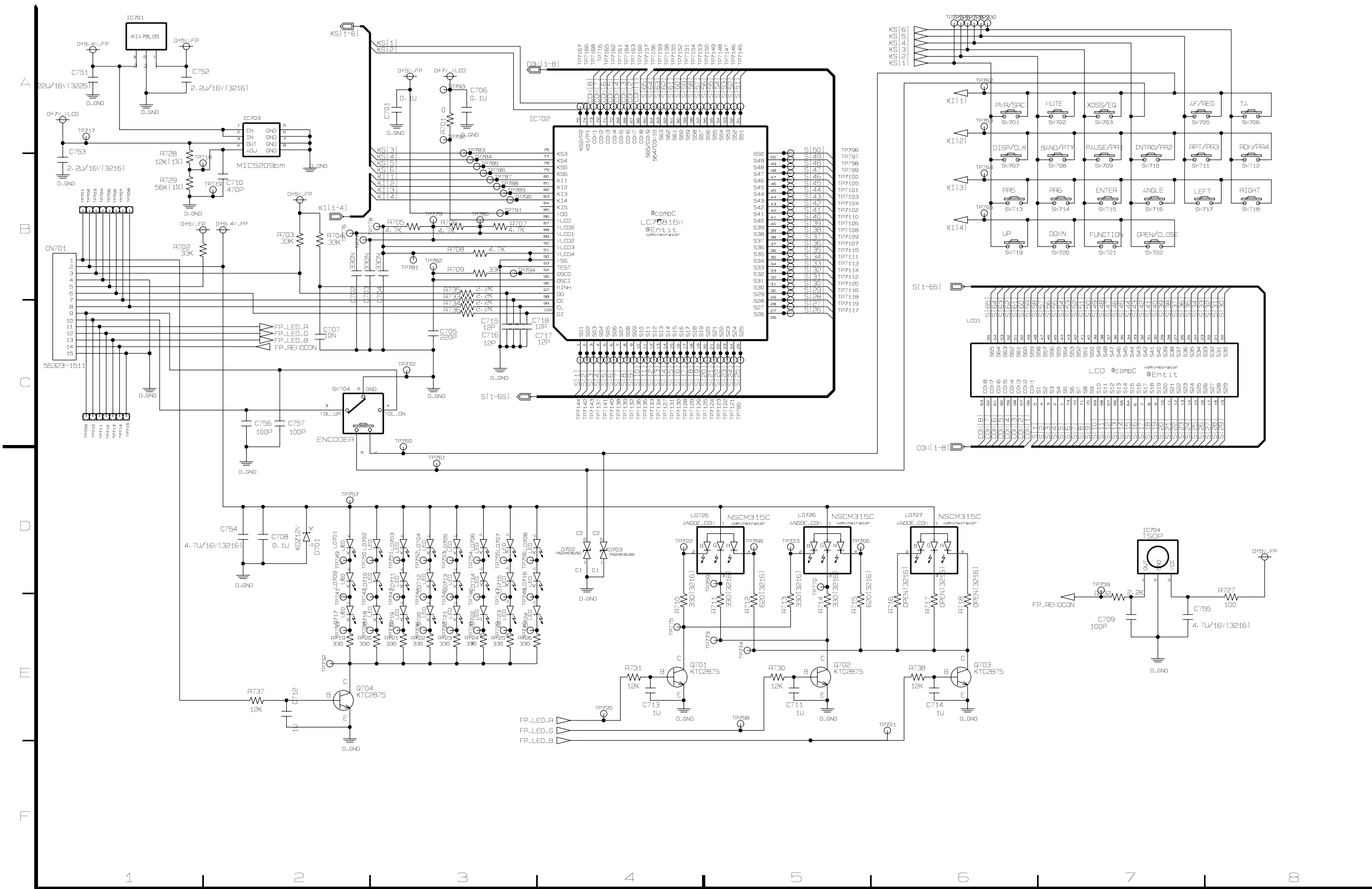


• POWER SCHEMATIC DIAGRAM

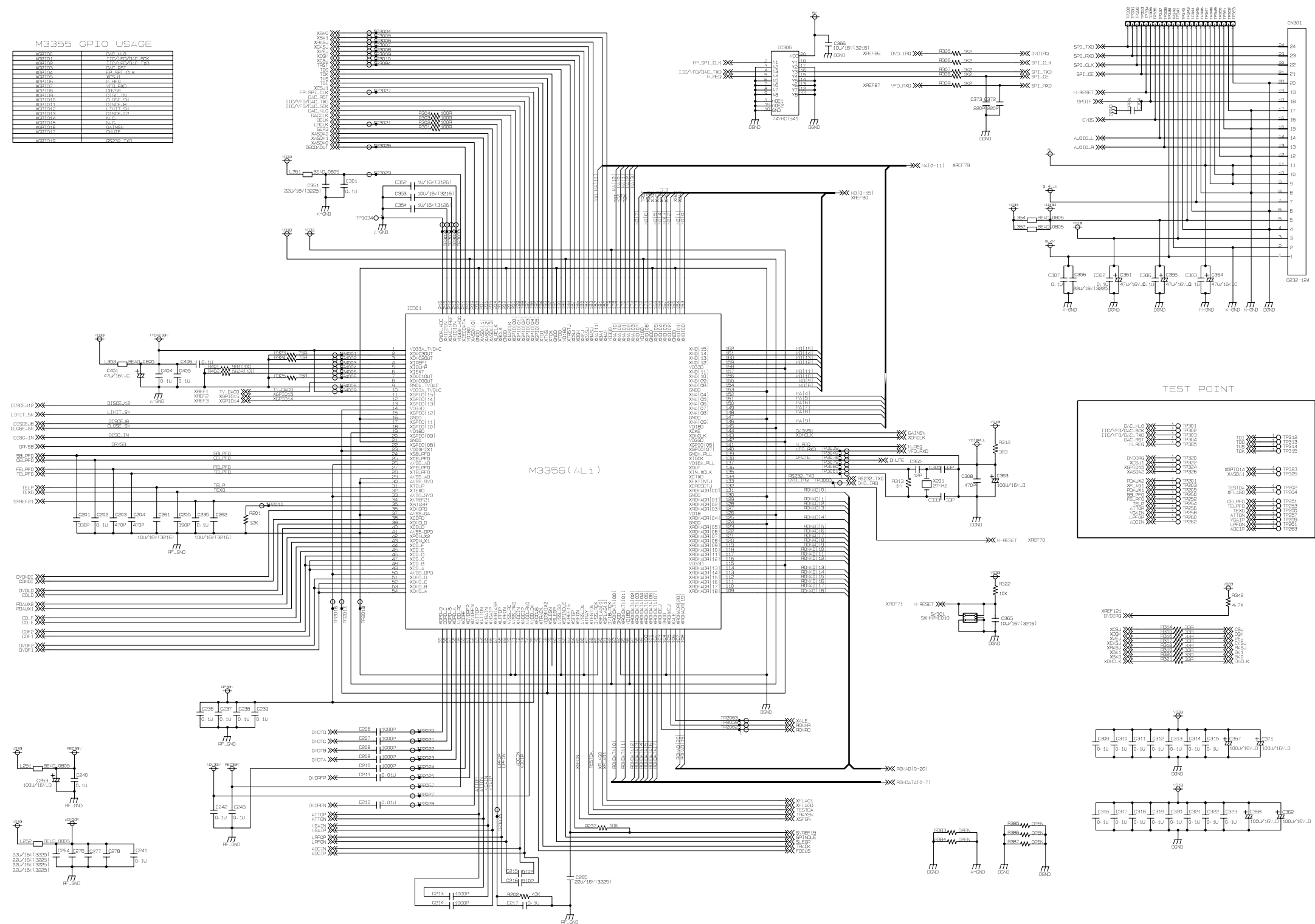


RECEIVER_MAIN BOARD 2004.08.25
SHEET 3 : POWER

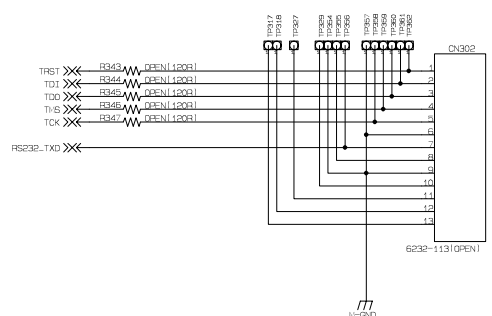
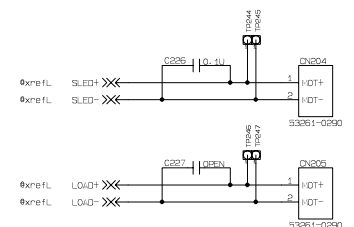
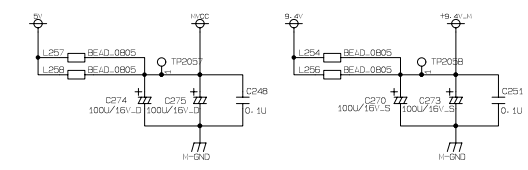
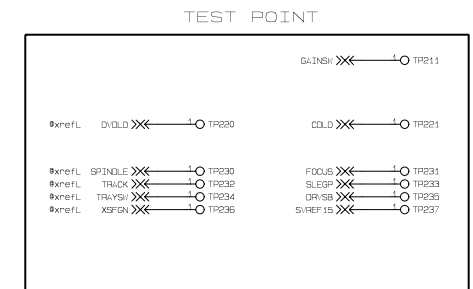
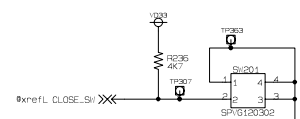
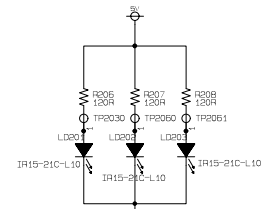
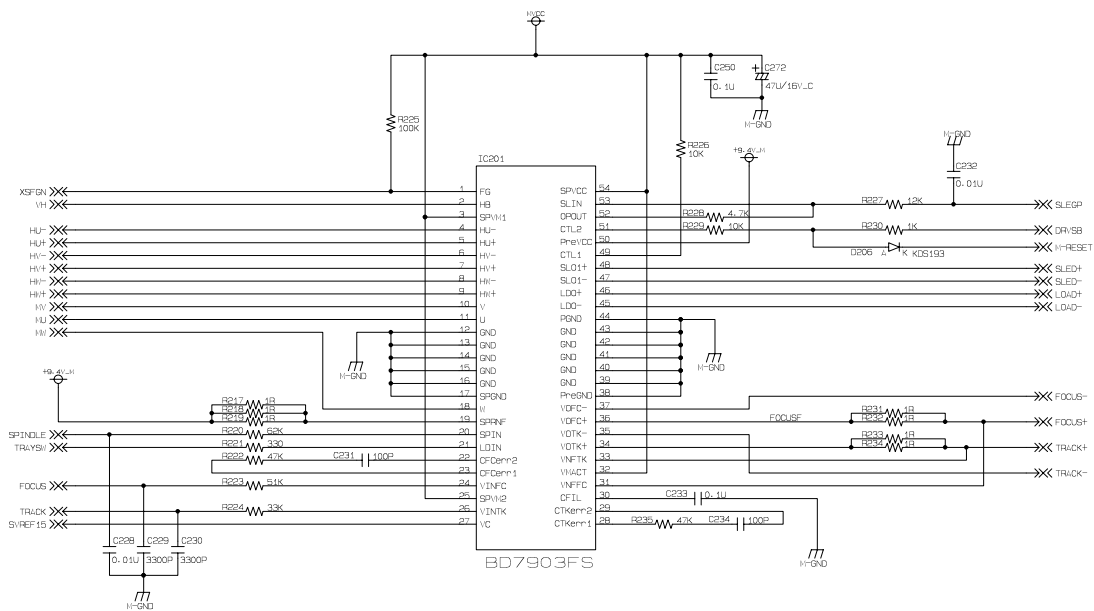
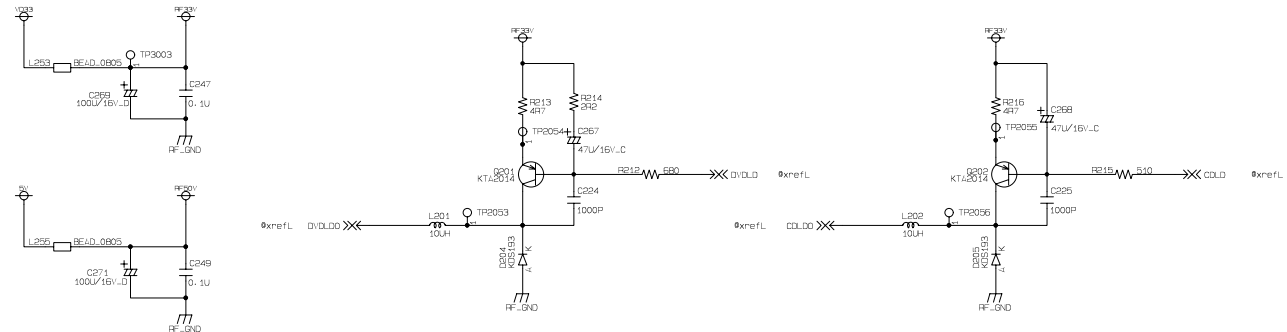
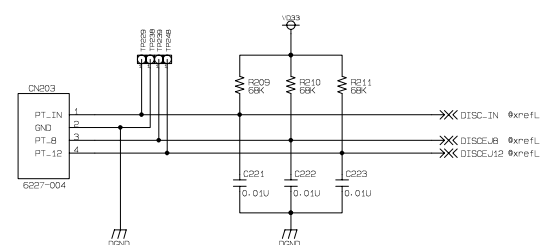
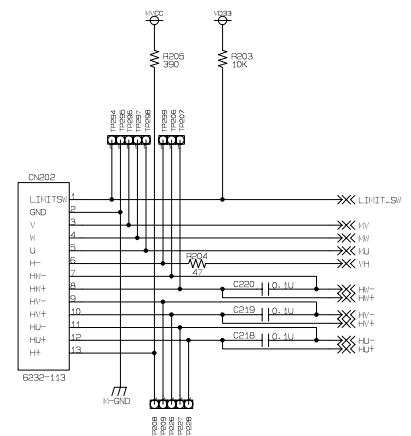
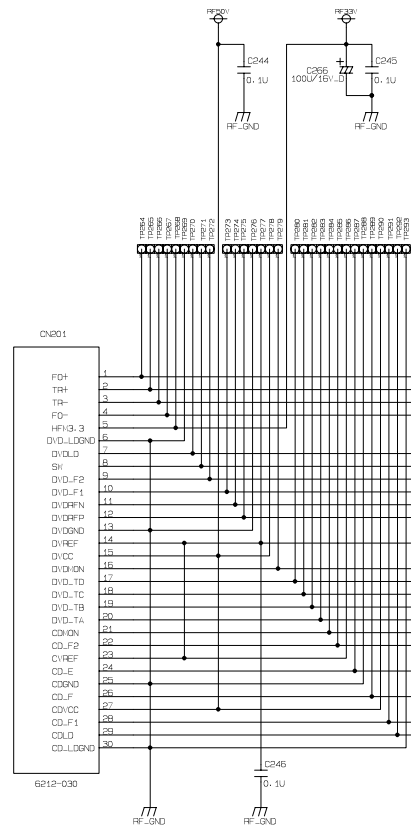
• FRONT SCHEMATIC DIAGRAM



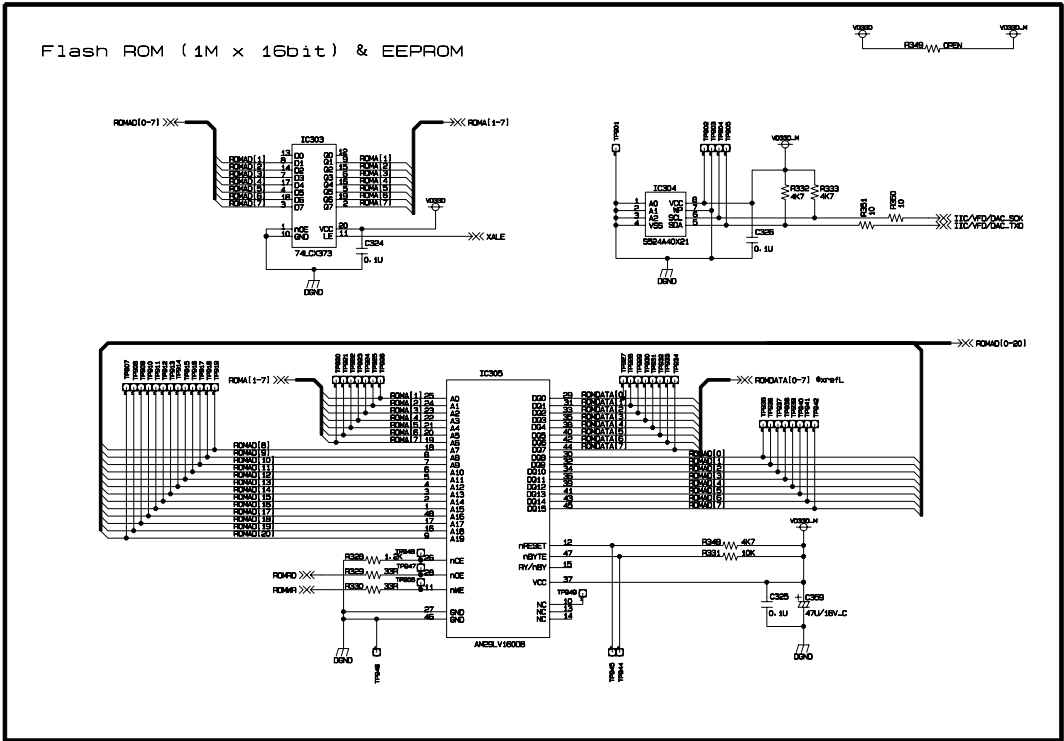
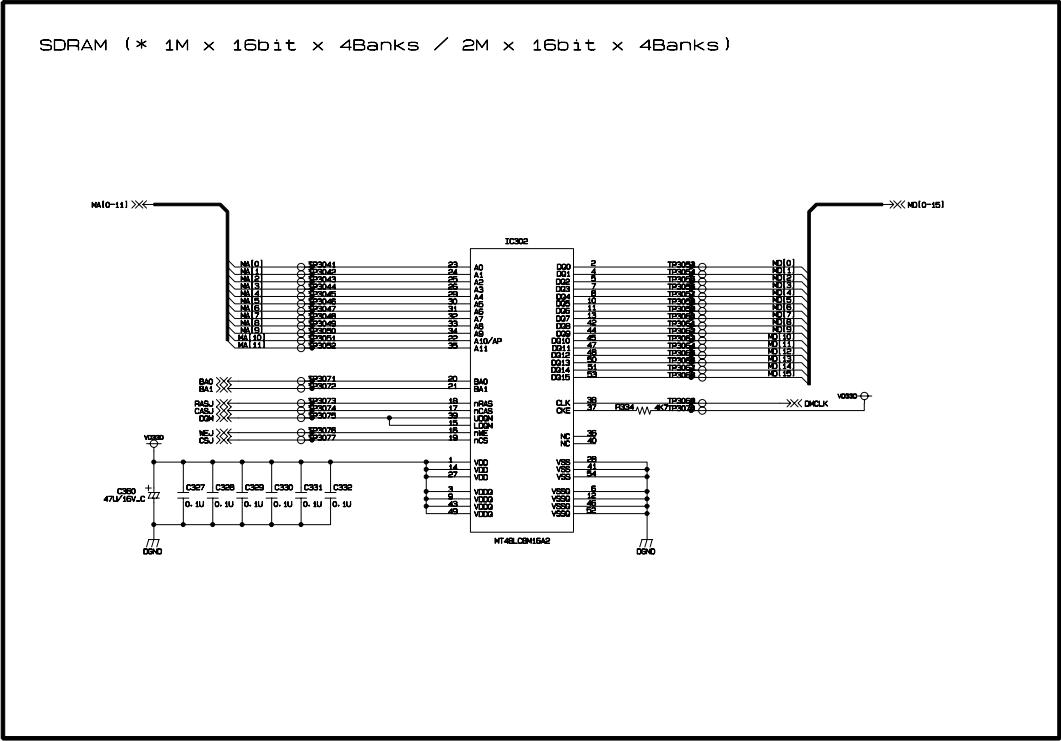
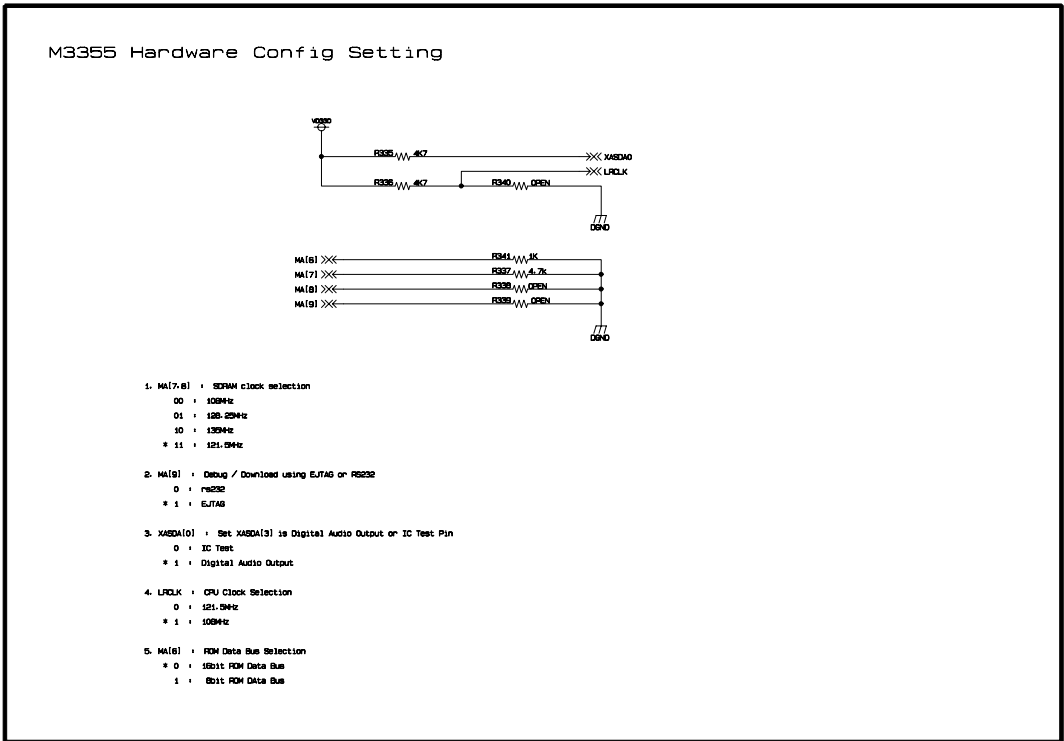
• DVD MPEG SCHEMATIC DIAGRAM



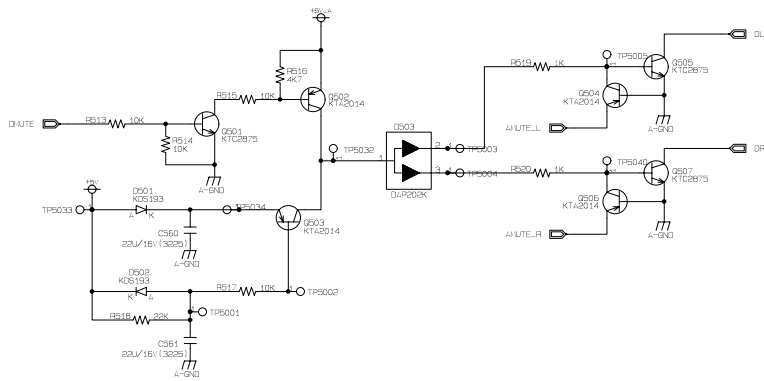
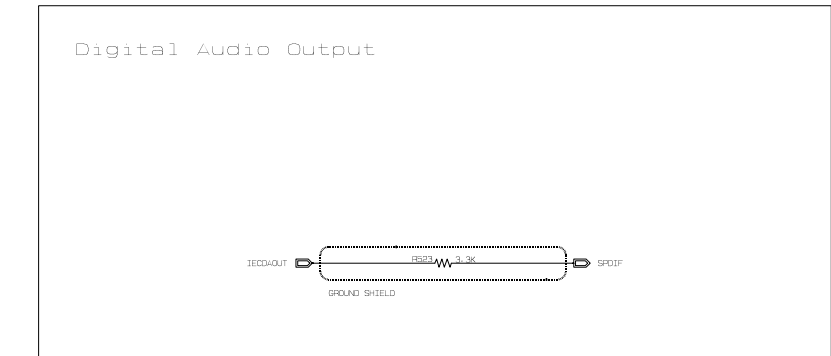
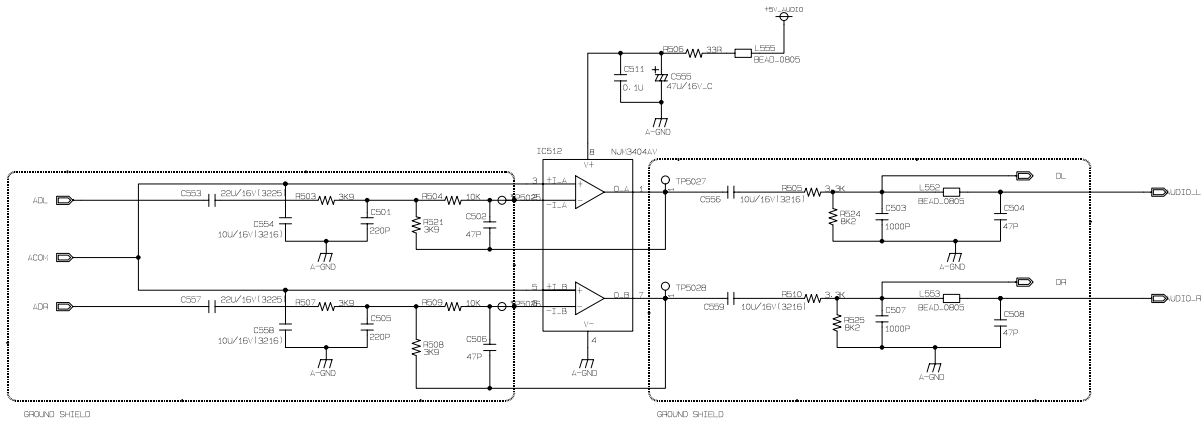
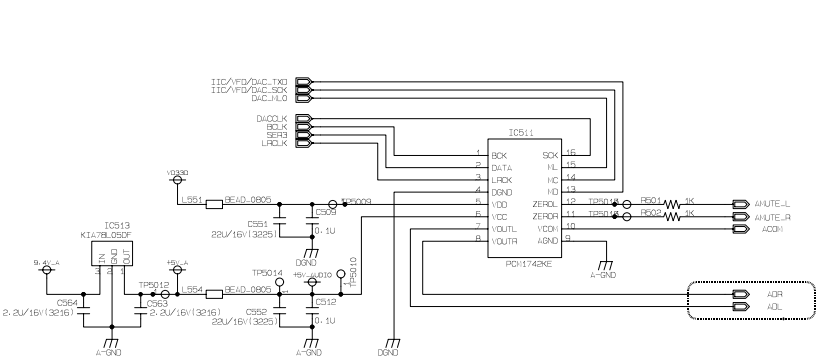
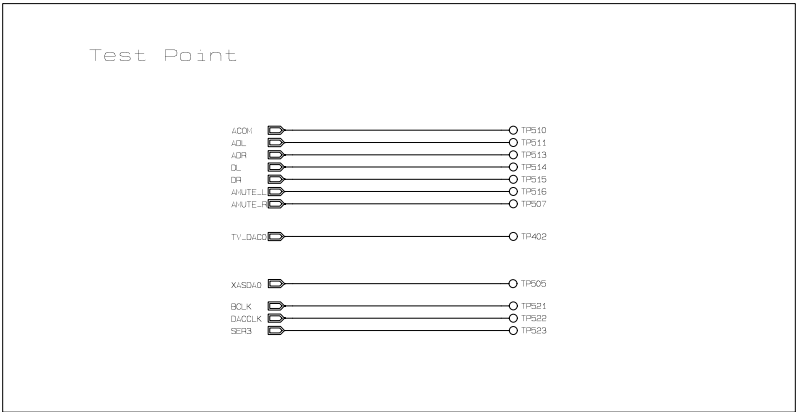
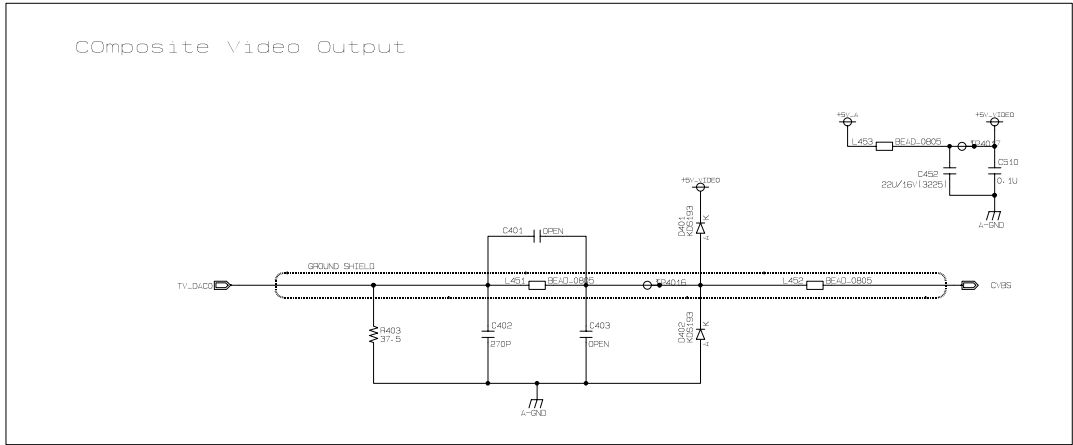
- **DVD SERVO SCHEMATIC DIAGRAM**



• DVD MEMORY SCHEMATIC DIAGRAM



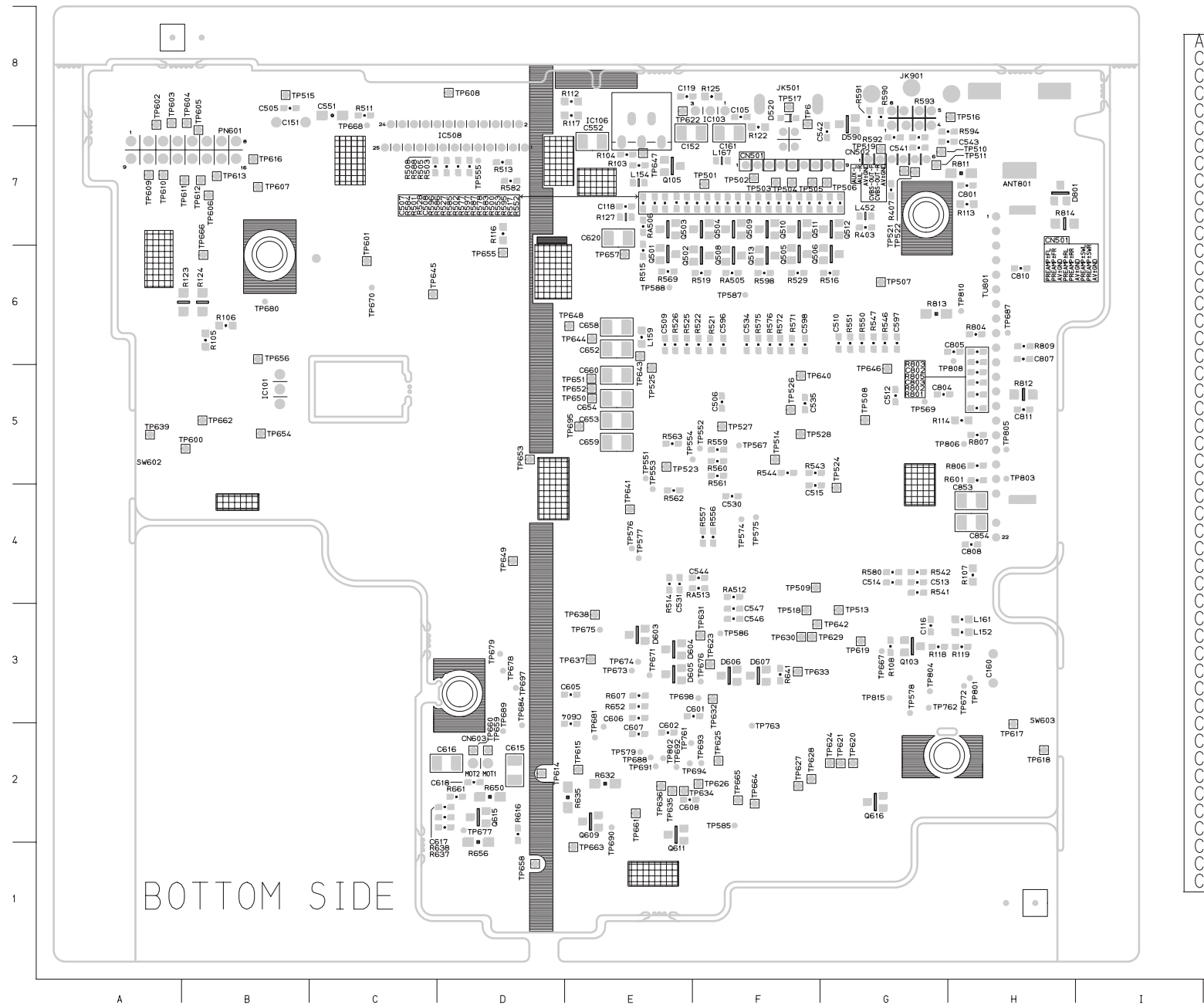
• DVD AV SCHEMATIC DIAGRAM



- **MAIN P.C. BOARD (TOP SIDE)**

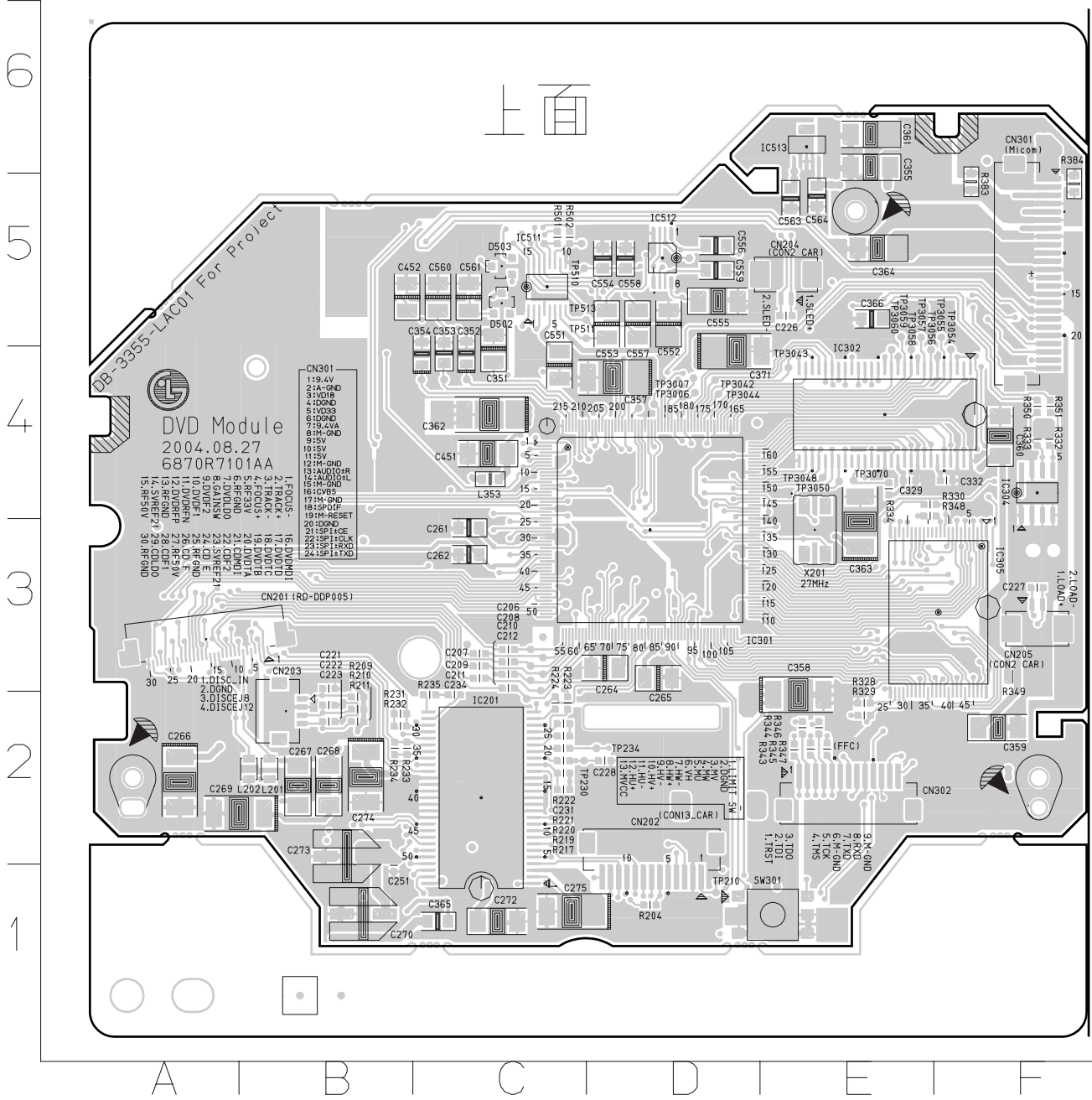
2-46

• MAIN P.C. BOARD (BOTTOM SIDE)



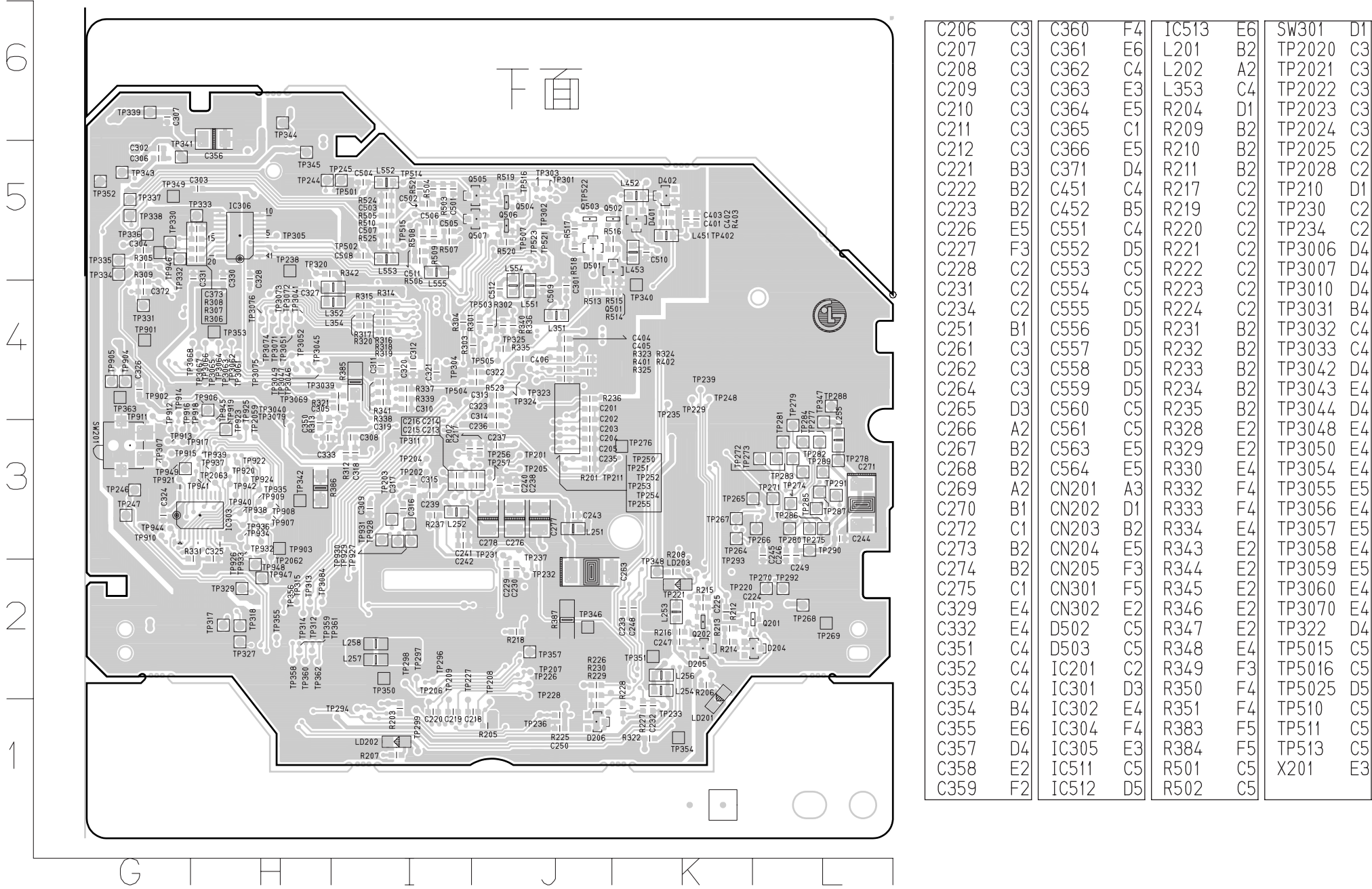
AN08012	C529	F603	G201	H101	I201	J301	K401	L501	M601	N701	O801	P901	Q101	R507	D2	R620	C2	
C102	C532	C609	D516	D517	D518	D519	D520	D521	D522	D523	D524	D525	Q106	F2	R509	D2	R621	C2
C103	C536	C610	E7	E8	F6	F6	F6	F6	F6	F6	F6	F6	Q109	I6	R510	F6	R622	B2
C104	C537	C611	G1	G1	G1	G1	G1	G1	G1	G1	G1	G1	Q401	G3	R512	D2	R623	B3
C106	C538	C612	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	Q402	E8	R520	D2	R624	B3
C107	C539	C614	B4	B4	B4	B4	B4	B4	B4	B4	B4	B4	Q403	G3	R523	F4	R625	B2
C108	C540	C640	H6	H6	H6	H6	H6	H6	H6	H6	H6	H6	Q404	G3	R524	F4	R626	B2
C114	C545	C651	E5	E5	E5	E5	E5	E5	E5	E5	E5	E5	Q405	G3	R530	H5	R627	B2
C115	C548	C655	D8	D8	D8	D8	D8	D8	D8	D8	D8	D8	Q406	G3	R531	G5	R628	F6
C120	C550	C656	G6	G6	G6	G6	G6	G6	G6	G6	G6	G6	Q407	G2	R532	G5	R629	H7
C121	C553	C657	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	Q408	F3	R533	G5	R630	B4
C122	C554	C661	F3	F3	F3	F3	F3	F3	F3	F3	F3	F3	Q409	G3	R534	G5	R631	E7
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C124	C557	C663	F4	F4	F4	F4	F4	F4	F4	F4	F4	F4	Q411	G2	R536	G5	R634	E7
C125	C558	C806	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	Q412	G3	R537	G5	R636	E7
C151	C559	C809	H3	H3	H3	H3	H3	H3	H3	H3	H3	H3	Q413	G2	R538	G5	R639	F6
C153	C560	C851	H2	H2	H2	H2	H2	H2	H2	H2	H2	H2	Q507	F6	R539	G5	R640	F6
C154	C561	C852	I3	I3	I3	I3	I3	I3	I3	I3	I3	I3	Q601	B2	R540	G4	R642	F6
C155	C562	CN501	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	Q602	B2	R545	G4	R643	F6
C156	C563	CN502	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	Q603	B2	R548	H4	R644	F6
C157	C564	CN601	E3	E3	E3	E3	E3	E3	E3	E3	E3	E3	Q604	E7	R549	G4	R645	F6
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C159	C566	CN603	D7	D7	D7	D7	D7	D7	D7	D7	D7	D7	Q606	E7	R555	F5	R647	F6
C160	C567	CN604	G7	G7	G7	G7	G7	G7	G7	G7	G7	G7	Q607	C3	R558	F5	R648	H6
C162	C568	CN605	F7	F7	F7	F7	F7	F7	F7	F7	F7	F7	Q608	E8	R564	F6	R649	B4
C401	C569	D101	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	Q610	E7	R565	F6	R651	H7
C402	C570	D103	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	Q612	E7	R566	F6	R653	F7
C451	C571	D104	C5	C5	C5	C5	C5	C5	C5	C5	C5	C5	Q614	E7	R567	F6	R654	F7
C452	C572	D105	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	R101	C3	R568	F6	R655	F7
C453	C573	D106	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	R102	C3	R570	G6	R657	E7
C454	C574	D110	B3	B3	B3	B3	B3	B3	B3	B3	B3	B3	R109	F2	R573	G4	R659	E7
C501	C575	D111	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	R110	E1	R574	G4	R660	F7
C502	C576	D404	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	R111	B3	R581	E2	R662	H7
C503	C577	D405	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	R115	H5	R602	F7	R663	C3
C504	C578	D501	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R120	F2	R603	F7	R664	F3
C511	C579	D502	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R121	F2	R604	F7	R665	C2
C516	C580	D503	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R401	G2	R605	F7	R810	H6
C517	C581	D504	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R402	G3	R606	F6	RA501	F2
C518	C582	D505	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R404	G2	R608	F6	RA502	F2
C519	C583	D506	D3	D3	D3	D3	D3	D3	D3	D3	D3	D3	R405	G2	R609	F7	SW601	E8
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C521	C585	D508	C3	C3	C3	C3	C3	C3	C3	C3	C3	C3	R408	H2	R611	F7	SW603	I6
C522	C586	D509	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	R409	G3	R612	E6	TUN80	H2
C523	C587	D510	H5	H5	H5	H5	H5	H5	H5	H5	H5	H5	R410	G2	R613	F7	X601	E6
C524	C588	D511	G4	G4	G4	G4	G4	G4	G4	G4	G4	G4	R411	G2	R614	E7		
C525	C589	D512	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	R412	G3	R615	E8		
C526	C590	D513	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	R413	B2	R617	E5		
C527	C591	D514	G2	G2	G2	G2	G2	G2	G2	G2	G2	G2	R504	D2	R618	G7		
C528	C595	D515	F2	F2	F2	F2	F2	F2	F2	F2	F2	F2	R506	D2	R619	B2		

• DVD P.C. BOARD (TOP SIDE)



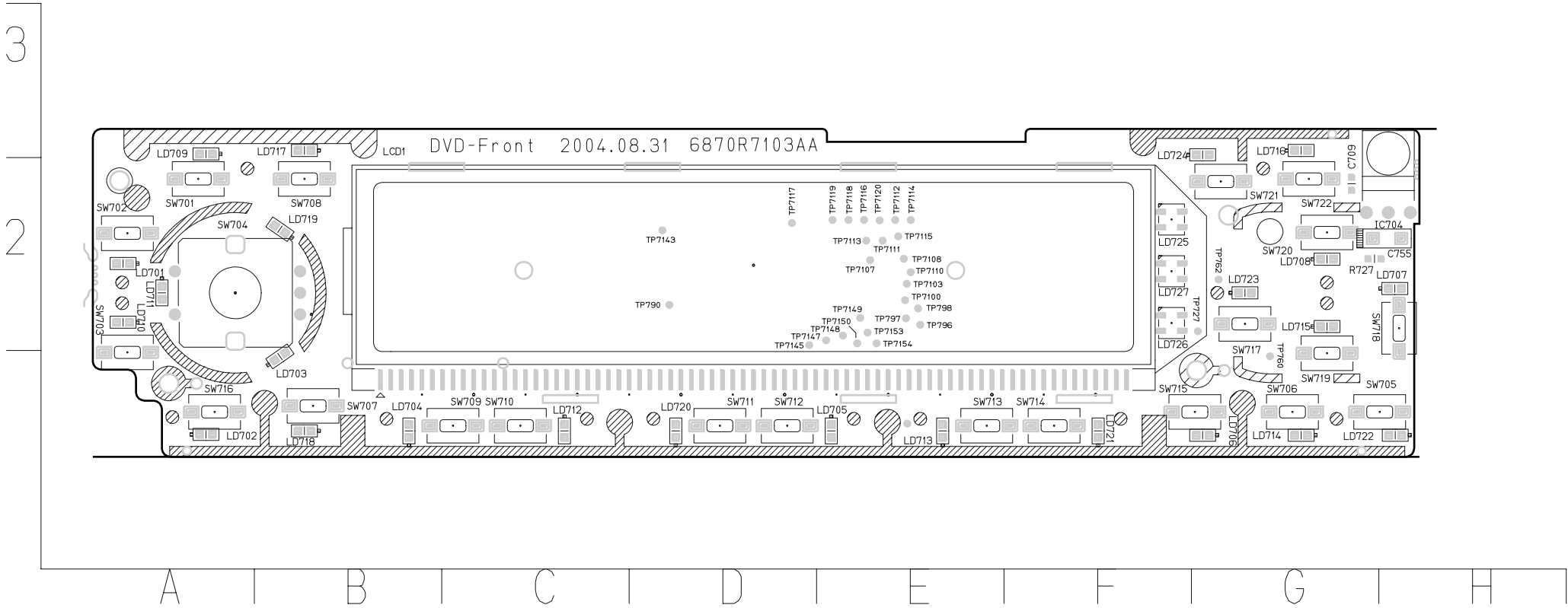
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C208	C3	C362	C4	L202	A2	TP2021	C3
C209	C3	C363	E3	L353	C4	TP2022	C3
C210	C3	C364	E5	R204	D1	TP2023	C3
C211	C3	C365	C1	R209	B2	TP2024	C3
C212	C3	C366	E5	R210	B2	TP2025	C2
C221	B3	C371	D4	R211	B2	TP2028	C2
C222	B2	C451	C4	R217	C2	TP210	D1
C223	B2	C452	B5	R219	C2	TP230	C2
C226	E5	C551	C4	R220	C2	TP234	C2
C227	F3	C552	D5	R221	C2	TP3006	D4
C228	C2	C553	C5	R222	C2	TP3007	D4
C231	C2	C554	C5	R223	C2	TP3010	D4
C234	C2	C555	D5	R224	C2	TP3031	B4
C251	B1	C556	D5	R231	B2	TP3032	C4
C261	C3	C557	D5	R232	B2	TP3033	C4
C262	C3	C558	D5	R233	B2	TP3042	D4
C264	C3	C559	D5	R234	B2	TP3043	E4
C265	D3	C560	C5	R235	B2	TP3044	D4
C266	A2	C561	C5	R328	E2	TP3048	E4
C267	B2	C563	E5	R329	E2	TP3050	E4
C268	B2	C564	E5	R330	E4	TP3054	E4
C269	A2	CN201	A3	R332	F4	TP3055	E5
C270	B1	CN202	D1	R333	F4	TP3056	E4
C272	C1	CN203	B2	R334	E4	TP3057	E5
C273	B2	CN204	E5	R343	E2	TP3058	E4
C274	B2	CN205	F3	R344	E2	TP3059	E5
C275	C1	CN301	F5	R345	E2	TP3060	E4
C329	E4	CN302	E2	R346	E2	TP3070	E4
C332	E4	D502	C5	R347	E2	TP322	D4
C351	C4	D503	C5	R348	E4	TP5015	C5
C352	C4	IC201	C2	R349	F3	TP5016	C5
C353	C4	IC301	D3	R350	F4	TP5025	D5
C354	B4	IC302	E4	R351	F4	TP510	C5
C355	E6	IC304	F4	R383	F5	TP511	C5
C357	D4	IC305	E3	R384	F5	TP513	C5
C358	E2	IC511	C5	R501	C5	X201	E3
C359	F2	IC512	D5	R502	C5		

• DVD P.C. BOARD (BOTTOM SIDE)



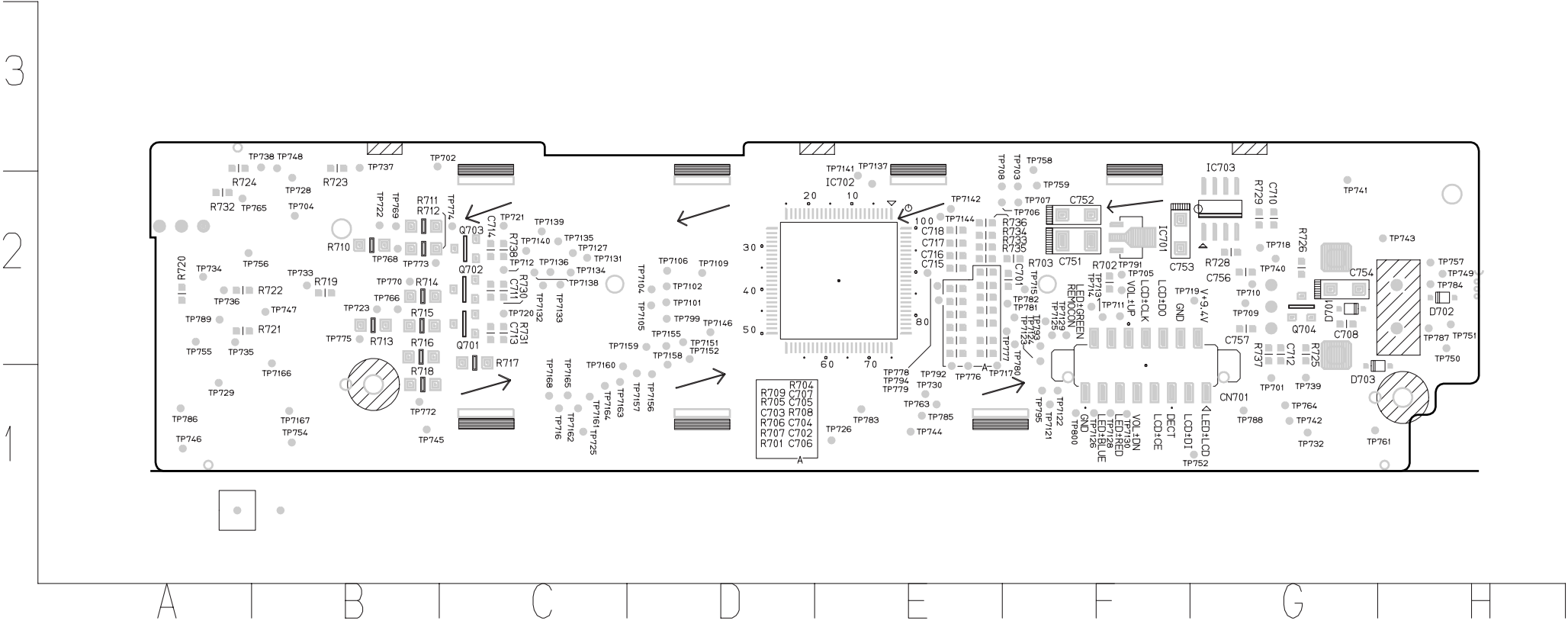
C206	C3	C360	F4	IC513	E6	SW301	D1
C207	C3	C361	E6	L201	B2	TP2020	C3
C208	C3	C362	C4	L202	A2	TP2021	C3
C209	C3	C363	E3	L353	C4	TP2022	C3
C210	C3	C364	E5	R204	D1	TP2023	C3
C211	C3	C365	C1	R209	B2	TP2024	C3
C212	C3	C366	E5	R210	B2	TP2025	C2
C221	B3	C371	D4	R211	B2	TP2028	C2
C222	B2	C451	C4	R217	C2	TP210	D1
C223	B2	C452	B5	R219	C2	TP230	C2
C226	E5	C551	C4	R220	C2	TP234	C2
C227	F3	C552	D5	R221	C2	TP3006	D4
C228	C2	C553	C5	R222	C2	TP3007	D4
C231	C2	C554	C5	R223	C2	TP3010	D4
C234	C2	C555	D5	R224	C2	TP3031	B4
C251	B1	C556	D5	R231	B2	TP3032	C4
C261	C3	C557	D5	R232	B2	TP3033	C4
C262	C3	C558	D5	R233	B2	TP3042	D4
C264	C3	C559	D5	R234	B2	TP3043	E4
C265	D3	C560	C5	R235	B2	TP3044	D4
C266	A2	C561	C5	R328	E2	TP3048	E4
C267	B2	C563	E5	R329	E2	TP3050	E4
C268	B2	C564	E5	R330	E4	TP3054	E4
C269	A2	CN201	A3	R332	F4	TP3055	E5
C270	B1	CN202	D1	R333	F4	TP3056	E4
C272	C1	CN203	B2	R334	E4	TP3057	E5
C273	B2	CN204	E5	R343	E2	TP3058	E4
C274	B2	CN205	F3	R344	E2	TP3059	E5
C275	C1	CN301	F5	R345	E2	TP3060	E4
C329	E4	CN302	E2	R346	E2	TP3070	E4
C332	E4	D502	C5	R347	E2	TP322	D4
C351	C4	D503	C5	R348	E4	TP5015	C5
C352	C4	IC201	C2	R349	F3	TP5016	C5
C353	C4	IC301	D3	R350	F4	TP5025	D5
C354	B4	IC302	E4	R351	F4	TP510	C5
C355	E6	IC304	F4	R383	F5	TP511	C5
C357	D4	IC305	E3	R384	F5	TP513	C5
C358	E2	IC511	C5	R501	C5	X201	E3
C359	F2	IC512	D5	R502	C5		

• FRONT P.C. BOARD (TOP SIDE)



C709	H2	SW712	E1
C755	H2	SW713	F1
IC704	H2	SW714	F1
LCD1	D2	SW715	G1
LD701	A2	SW716	B1
LD702	B1	SW717	G2
LD703	B1	SW718	H2
LD704	C1	SW719	H1
LD705	E1	SW720	H2
LD706	G1	SW721	G2
LD707	H2	SW722	G2
LD708	H2	TP7100	E2
LD709	B3	TP7103	E2
LD710	A2	TP7107	E2
LD711	A2	TP7108	E2
LD712	C1	TP7110	E2
LD713	E1	TP7111	E2
LD714	G1	TP7112	E2
LD715	H2	TP7113	E2
LD716	G3	TP7114	E2
LD717	B3	TP7115	E2
LD718	B1	TP7116	E2
LD719	B2	TP7117	E2
LD720	D1	TP7118	E2
LD721	F1	TP7119	E2
LD722	H1	TP7120	E2
LD723	G2	TP7143	D2
LD724	G3	TP7145	E2
LD725	G2	TP7147	E2
LD726	G2	TP7148	E2
LD727	G2	TP7149	E2
R727	H2	TP7150	E2
SW701	B2	TP7153	E2
SW702	A2	TP7154	E2
SW703	A1	TP727	G2
SW704	B2	TP753	E1
SW705	H1	TP760	G1
SW706	G1	TP762	G2
SW707	B1	TP790	D2
SW708	B2	TP796	E2
SW709	C1	TP797	E2
SW710	C1	TP798	E2
SW711	D1		

• FRONT P.C. BOARD (BOTTOM SIDE)



C709	H2	SW712	E1
C755	H2	SW713	F1
IC704	H2	SW714	F1
LCD1	D2	SW715	G1
LD701	A2	SW716	B1
LD702	B1	SW717	G2
LD703	B1	SW718	H2
LD704	C1	SW719	H1
LD705	E1	SW720	H2
LD706	G1	SW721	G2
LD707	H2	SW722	G2
LD708	H2	TP7100	E2
LD709	B3	TP7103	E2
LD710	A2	TP7107	E2
LD711	A2	TP7108	E2
LD712	C1	TP7110	E2
LD713	E1	TP7111	E2
LD714	G1	TP7112	E2
LD715	H2	TP7113	E2
LD716	G3	TP7114	E2
LD717	B3	TP7115	E2
LD718	B1	TP7116	E2
LD719	B2	TP7117	E2
LD720	D1	TP7118	E2
LD721	F1	TP7119	E2
LD722	H1	TP7120	E2
LD723	G2	TP7143	D2
LD724	G3	TP7145	E2
LD725	G2	TP7147	E2
LD726	G2	TP7148	E2
LD727	G2	TP7149	E2
R727	H2	TP7150	E2
SW701	B2	TP7153	E2
SW702	A2	TP7154	E2
SW703	A1	TP727	G2
SW704	B2	TP753	E1
SW705	H1	TP760	G1
SW706	G1	TP762	G2
SW707	B1	TP790	D2
SW708	B2	TP796	E2
SW709	C1	TP797	E2
SW710	C1	TP798	E2
SW711	D1		

CABINET AND MAIN FRAME SECTION

